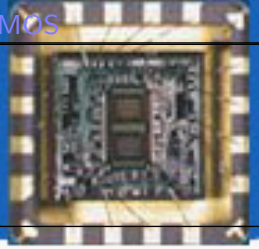


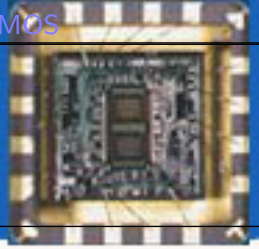
MOSFET Transistor

Structure and I/V Characteristics

Dr. Alaa El-Din Hussein

March 21, 2008

Outline



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4 Depletion NMOS Transistor

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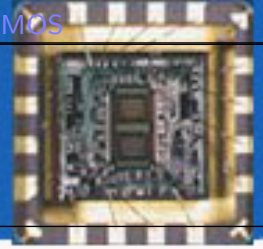

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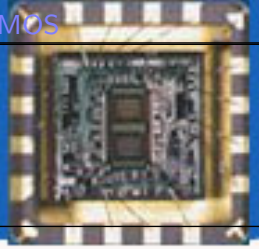

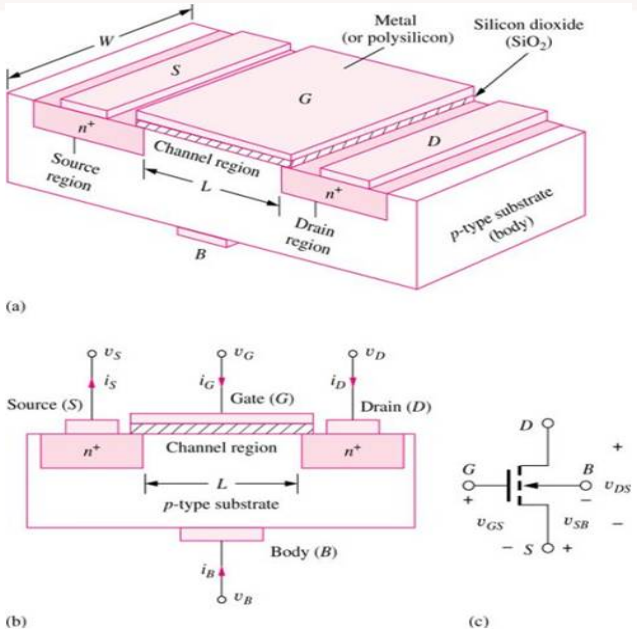

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- 4 device terminals: Gate(G), Drain(D), Source(S) and Body(B).
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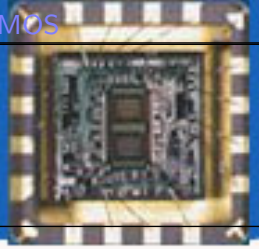

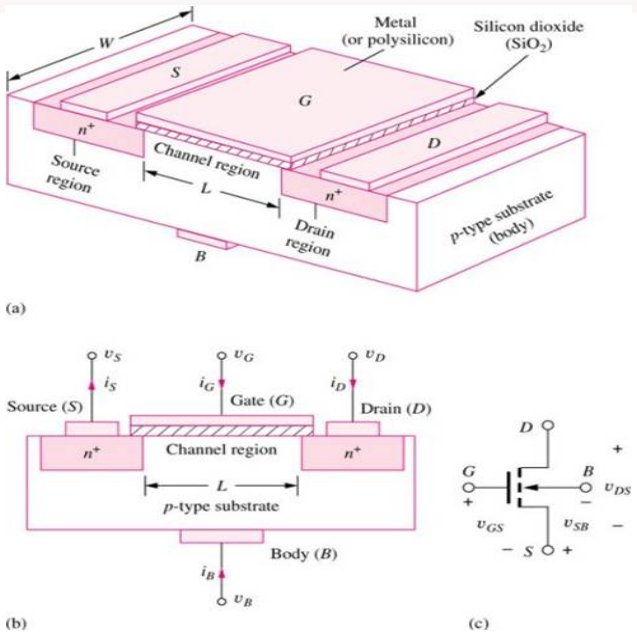

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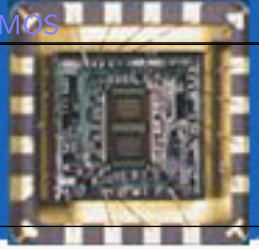

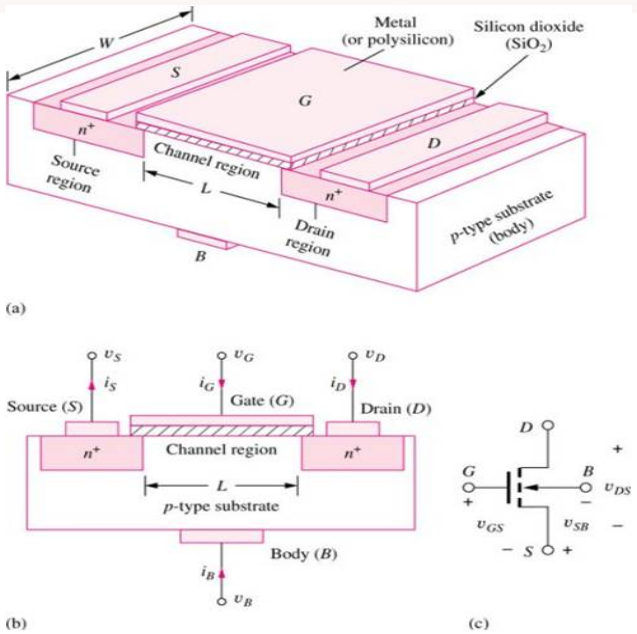

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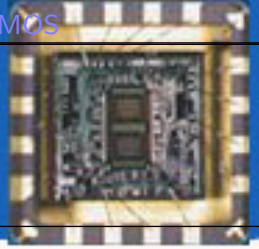

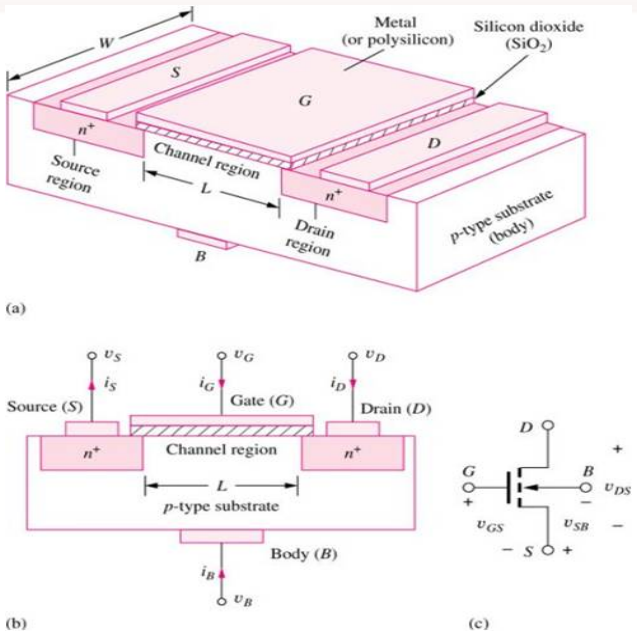

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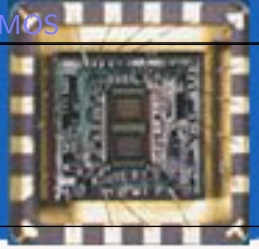

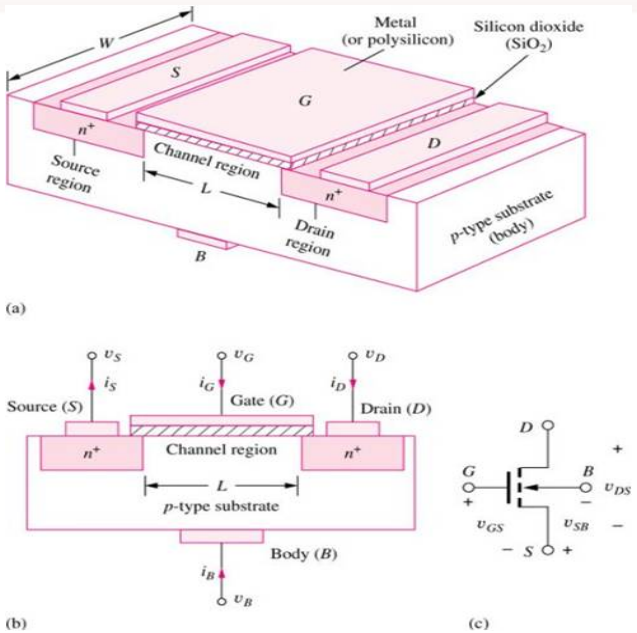

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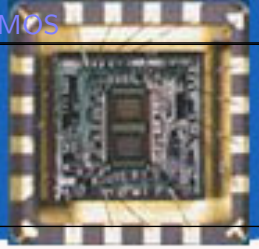

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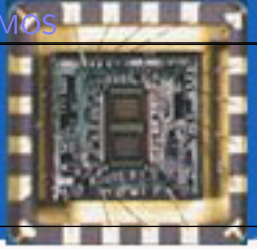
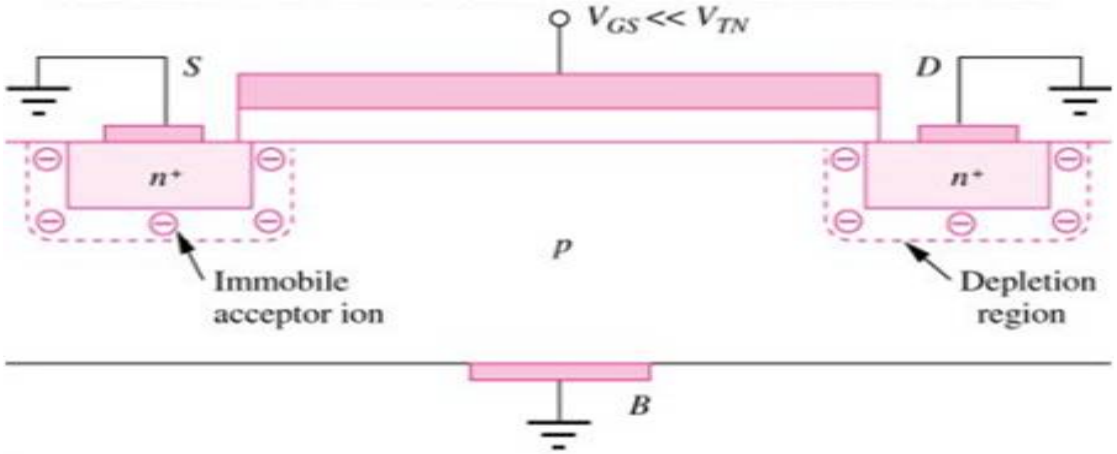
Qualitative I/V Characteristics

Gate Voltage equals zero





Notes

- $V_{GS} << V_{TN}$ (Threshold Voltage): Two back-to-back diodes exists in series between source and drain. Only small leakage current flows.
- Please note: In the text-book V_t is used for the threshold voltage to avoid confusion with the thermal voltage (V_T). We will use either V_t or(V_{TN} (n-device) and V_{TP} (P device))
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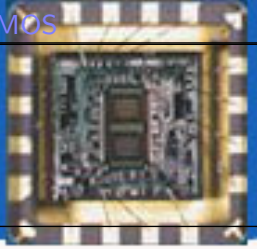

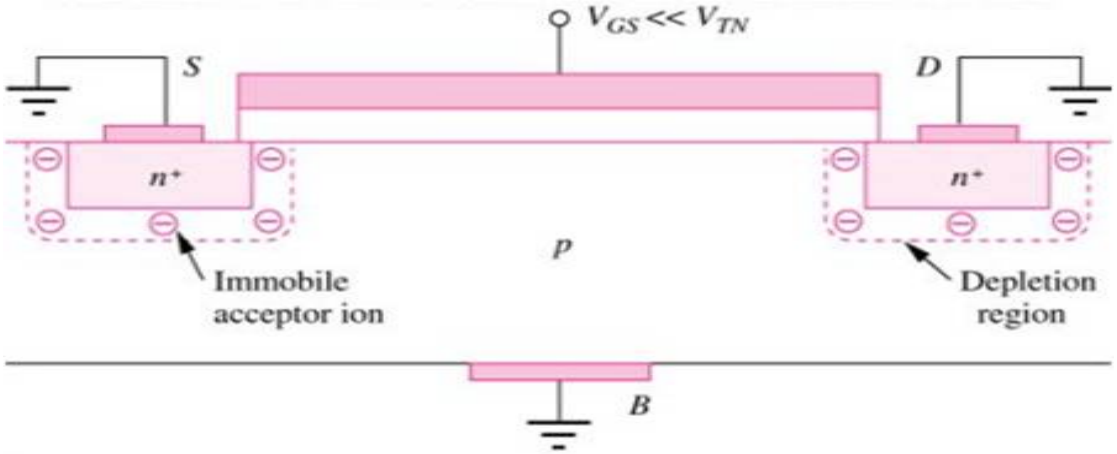

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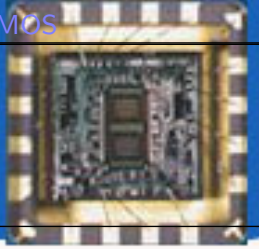

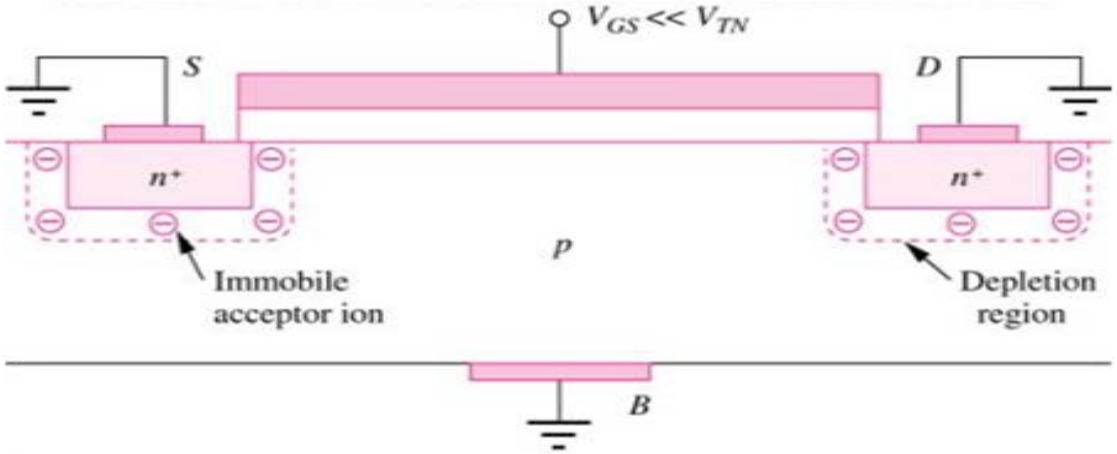

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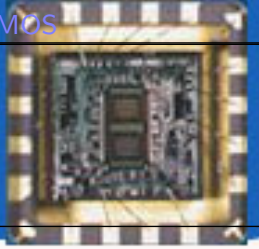

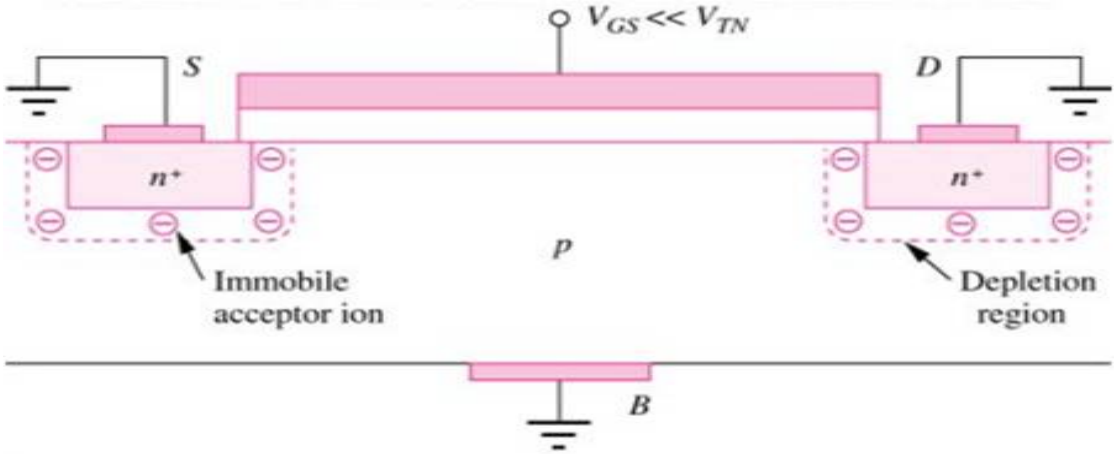

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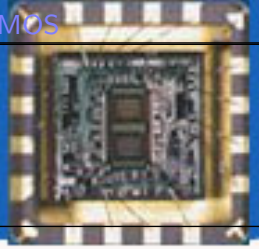

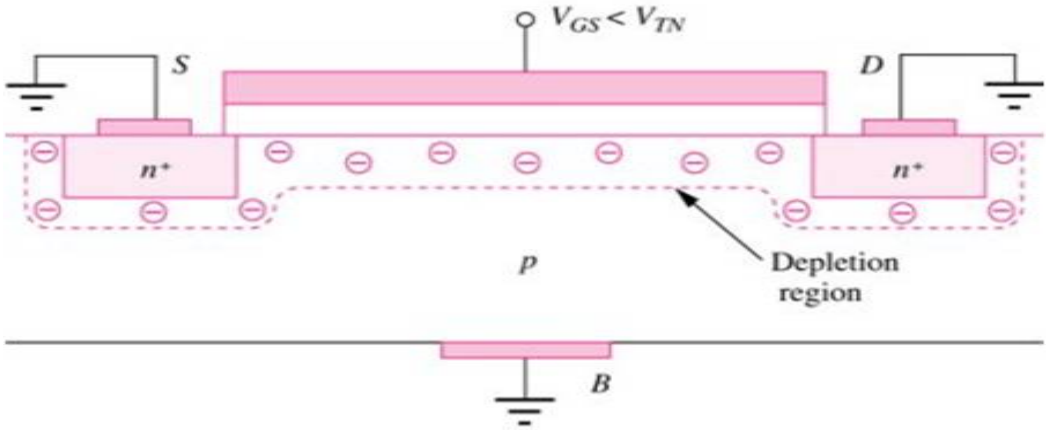

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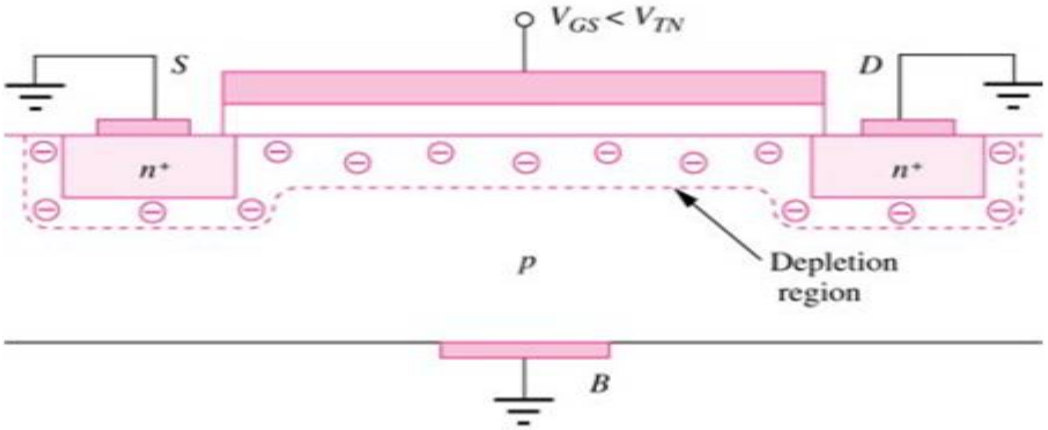

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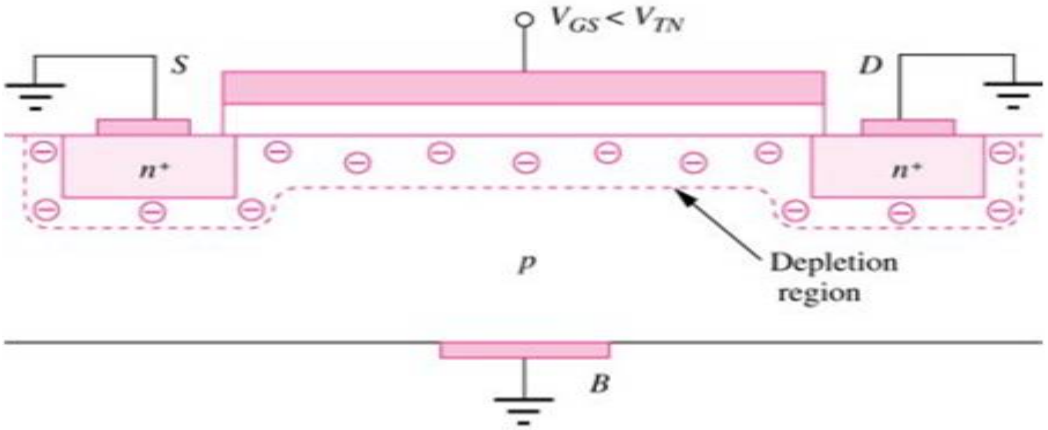

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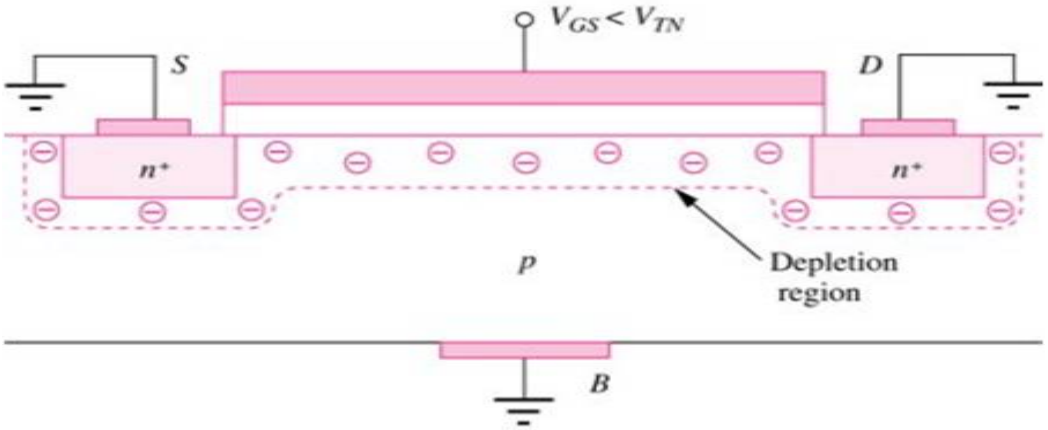

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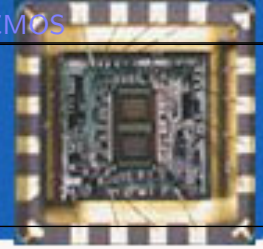

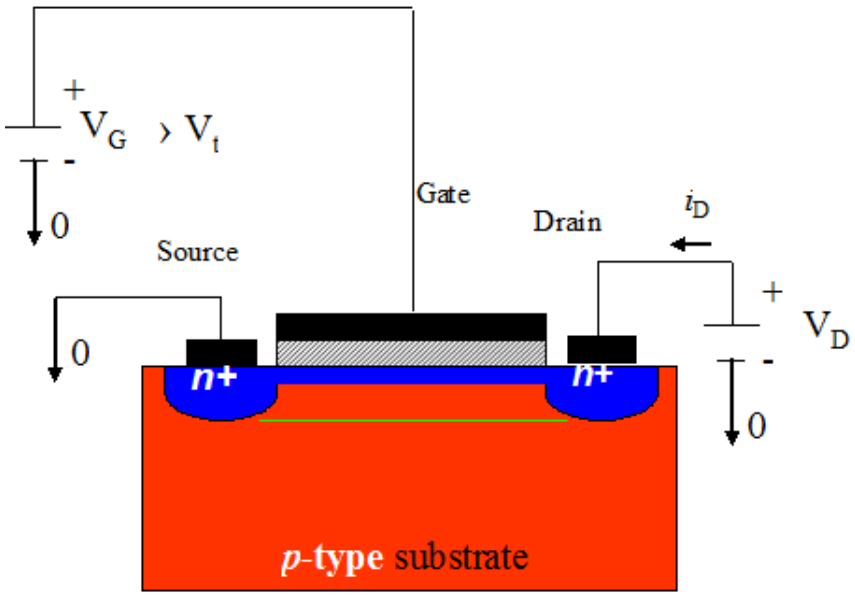

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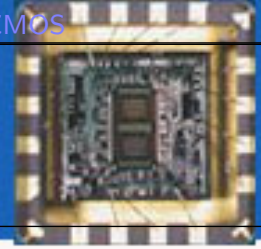

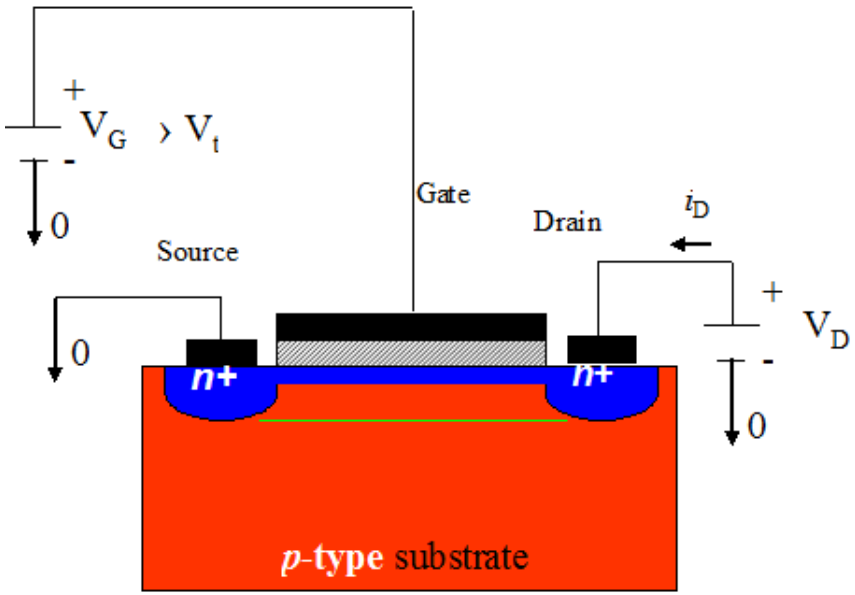

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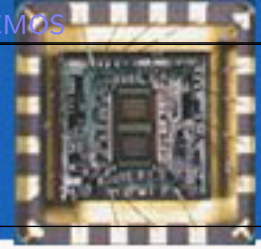

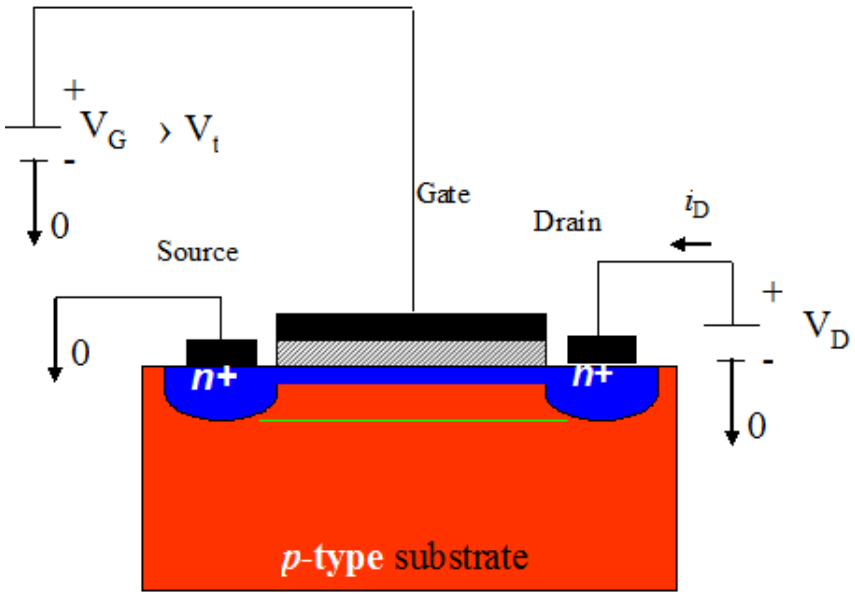

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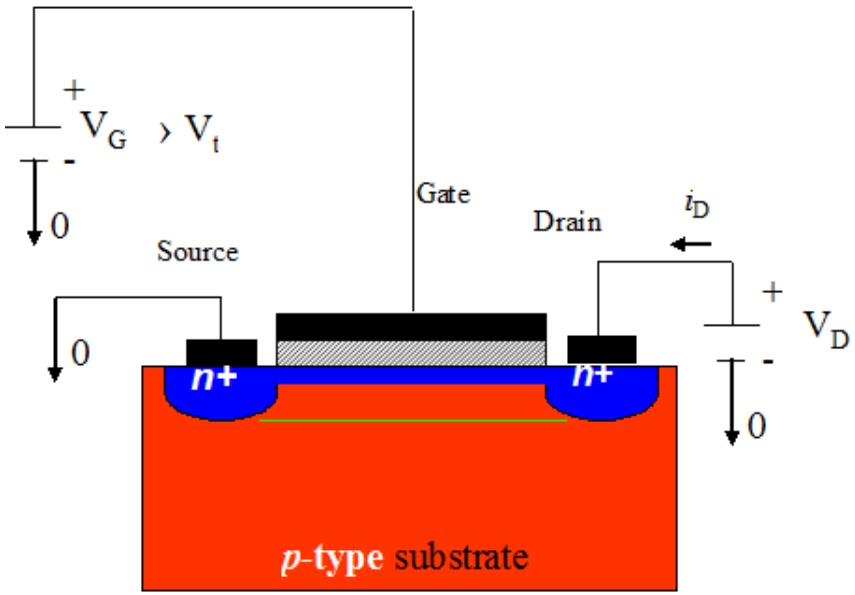

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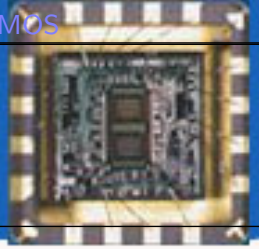

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NMOS Enhancement I/V Characteristics

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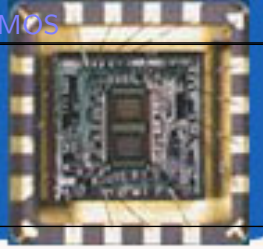

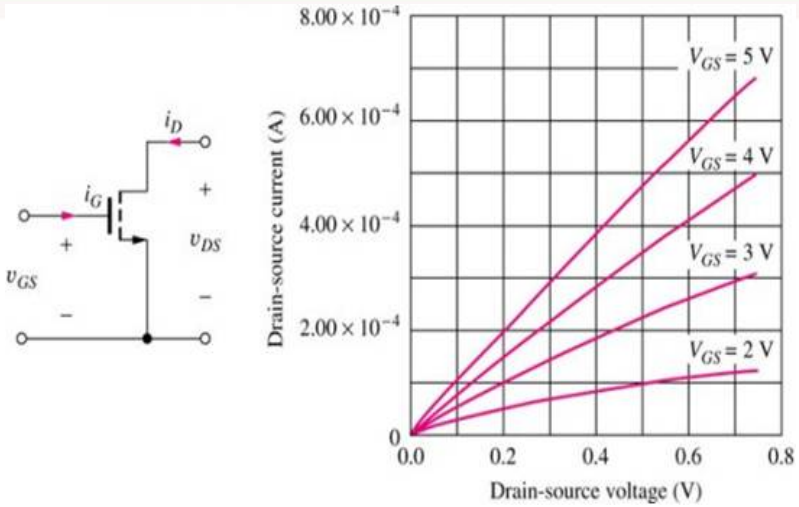

- $$i_D = K_n \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$

  where, $K_n = K_n' W/L$, $K_n' = \mu_n C_{ox} (A/V^2)$, $C_{ox} = \epsilon_{ox}/T_{ox}$, ϵ_{ox} =oxide permittivity (F/cm), T_{ox}=oxide thickness (cm)
- Channel current is drift
- Output characteristics appear to be linear.
- FET behaves like a gate-source voltage-controlled resistor between source and drain with $R_{on} = \frac{1}{K_n' \frac{W}{L} (V_{GS} - V_{TN})}$

NMOS Enhancement I/V Characteristics

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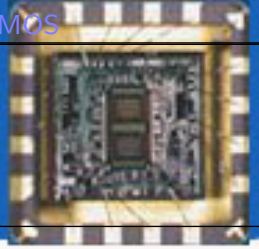

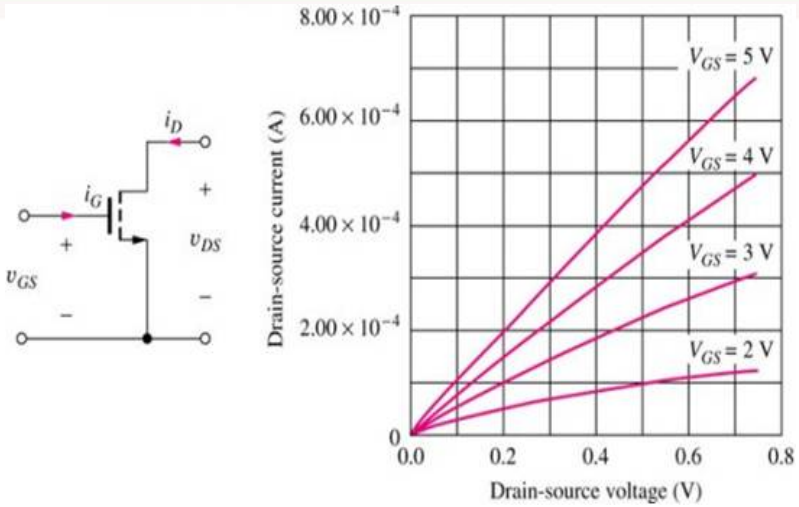

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NMOS Enhancement I/V Characteristics

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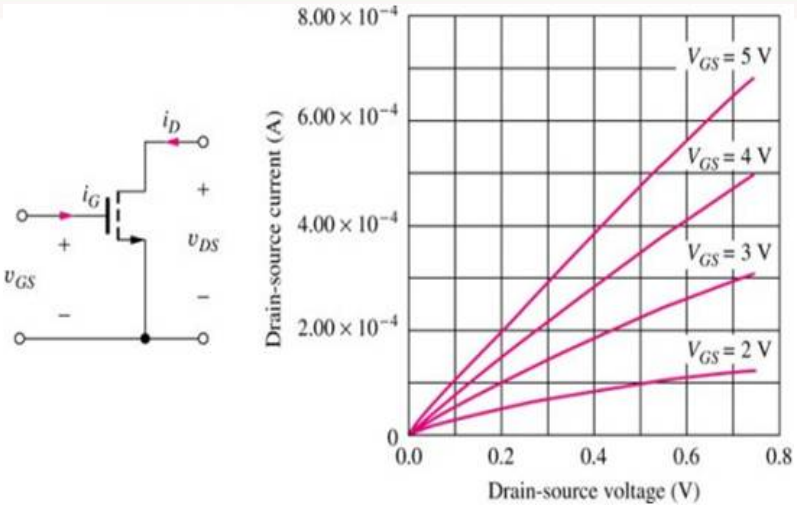

$$i_D = K_n \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$

where, $K_n = K_n' W/L$, $K_n' = \mu_n C_{ox} (A/V^2)$, $C_{ox} = \epsilon_{ox} / T_{ox}$, ϵ_{ox} =oxide permittivity (F/cm), T_{ox}=oxide thickness (cm)

- Channel current is drift
- Output characteristics appear to be linear.
- FET behaves like a gate-source voltage-controlled resistor between source and drain with $R_{on} = \frac{1}{K_n' \frac{W}{L} (V_{GS} - V_{TN})}$

NMOS Enhancement I/V Characteristics

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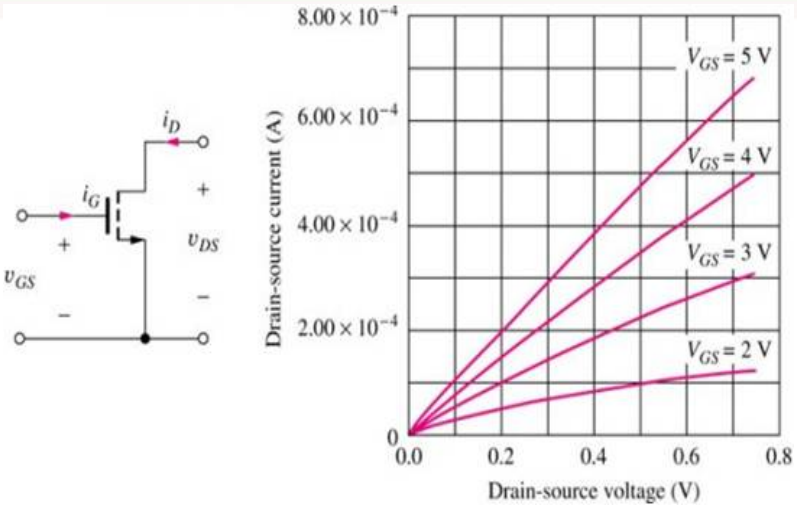

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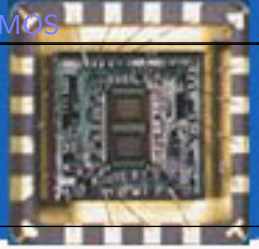

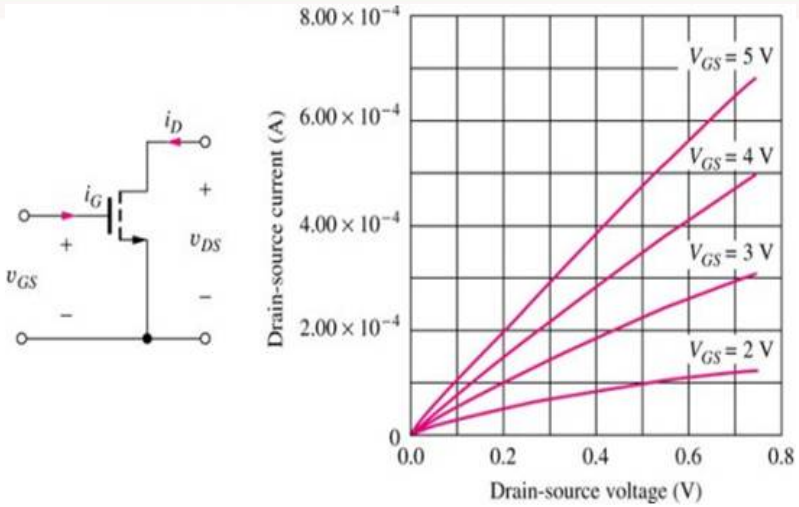

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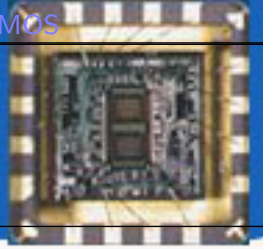
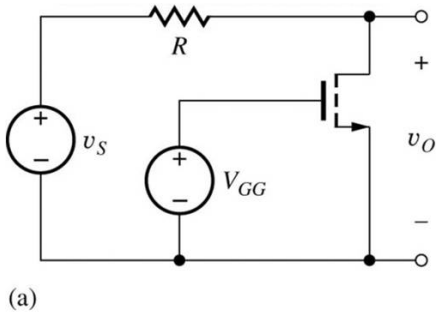
NMOS Enhancement I/V Characteristics

Example: Voltage-Controlled Attenuator





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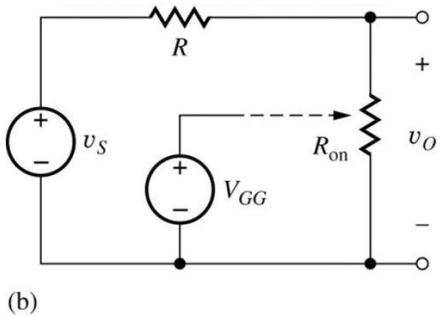

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Example

- Calculate v_o, given $K_n = 500\mu A/V^2, V_{TN} = 1V, R = 2k\Omega, V_{GG} = 1.5V$ and $v_s = 0.5V$
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NMOS Enhancement I/V Characteristics

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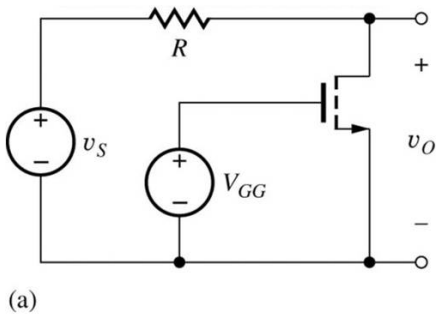

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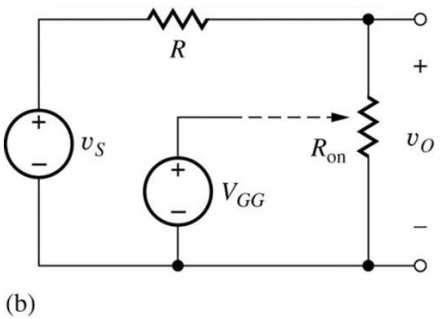

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NMOS Enhancement I/V Characteristics

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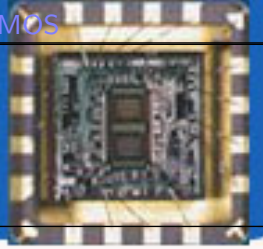

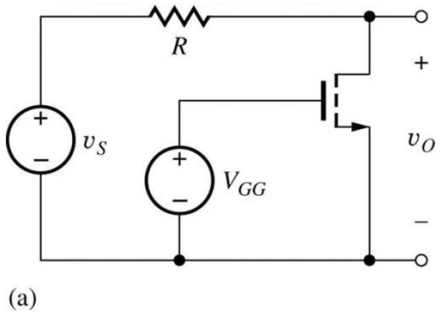

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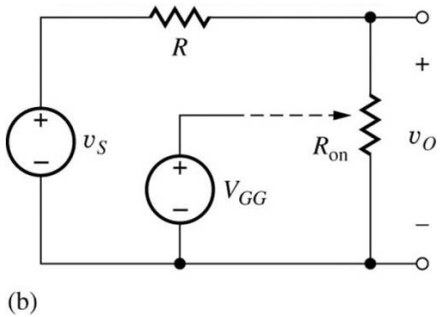

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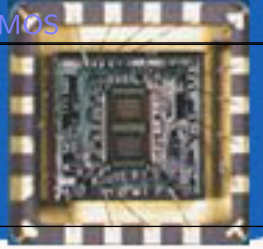

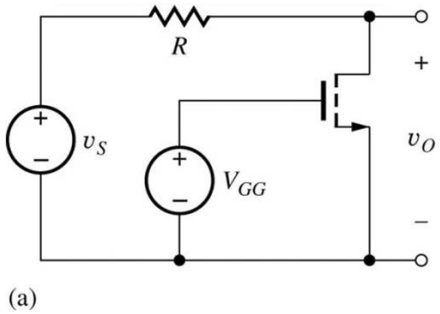

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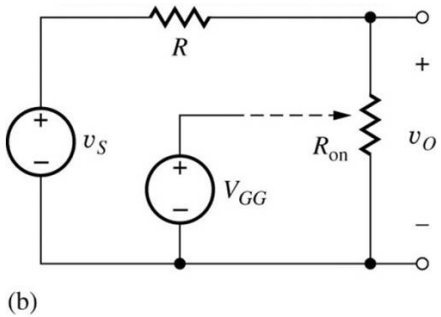

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NMOS Enhancement I/V Characteristics

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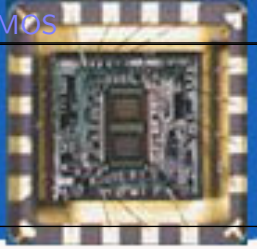

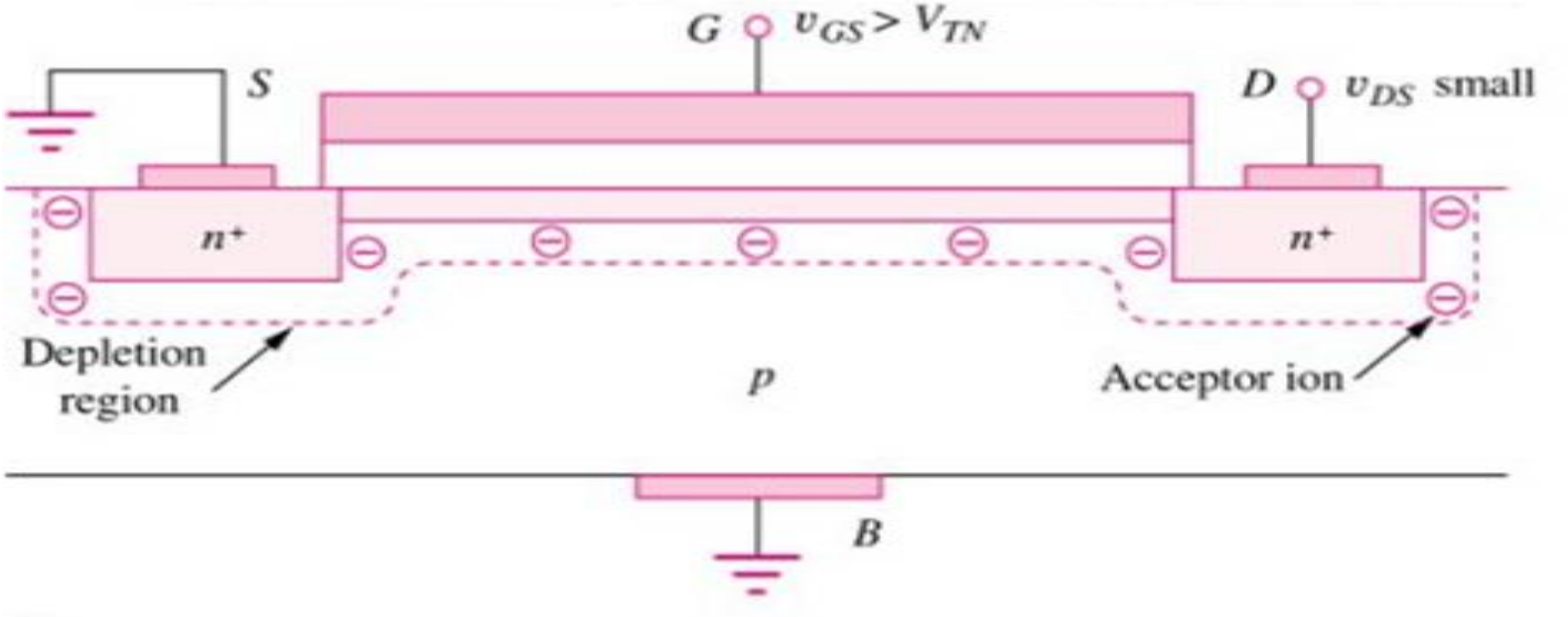

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NMOS Enhancement I/V Characteristics

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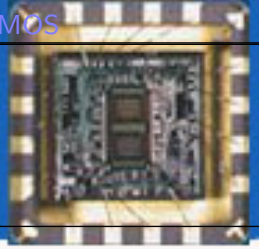

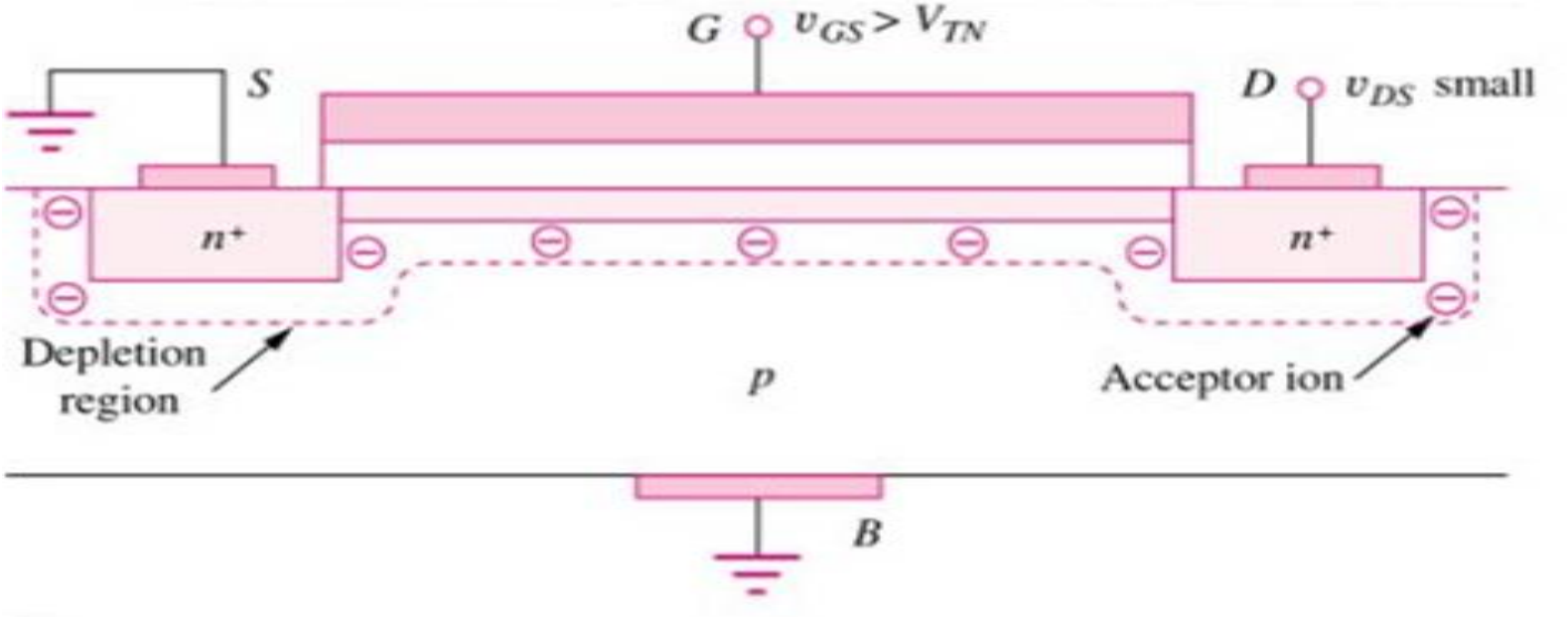

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NMOS Enhancement I/V Characteristics

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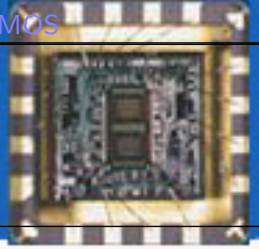

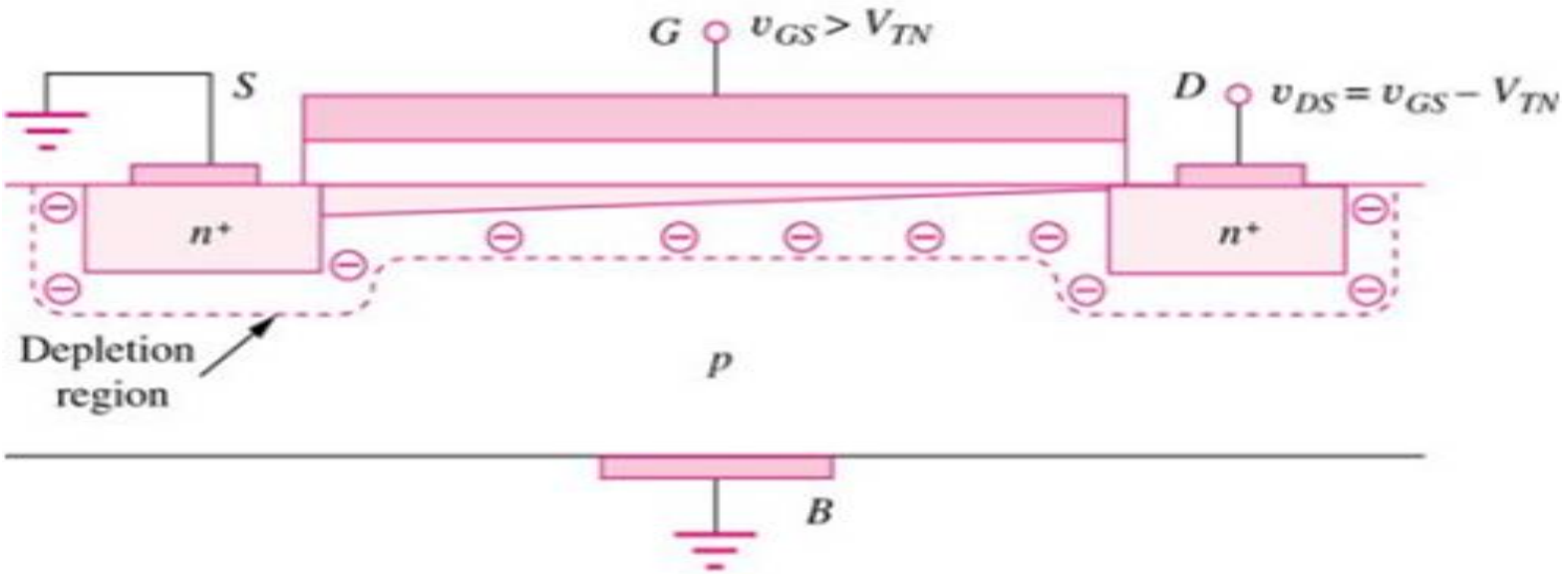

- If V_{DS} is increased the channel (inversion layer) will be tapered near the drain and it will disappear when $V_{DS} = V_{Dsat} = V_{GS} - V_{TN}$.

NMOS Enhancement I/V Characteristics

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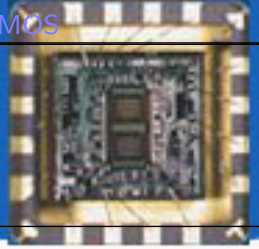

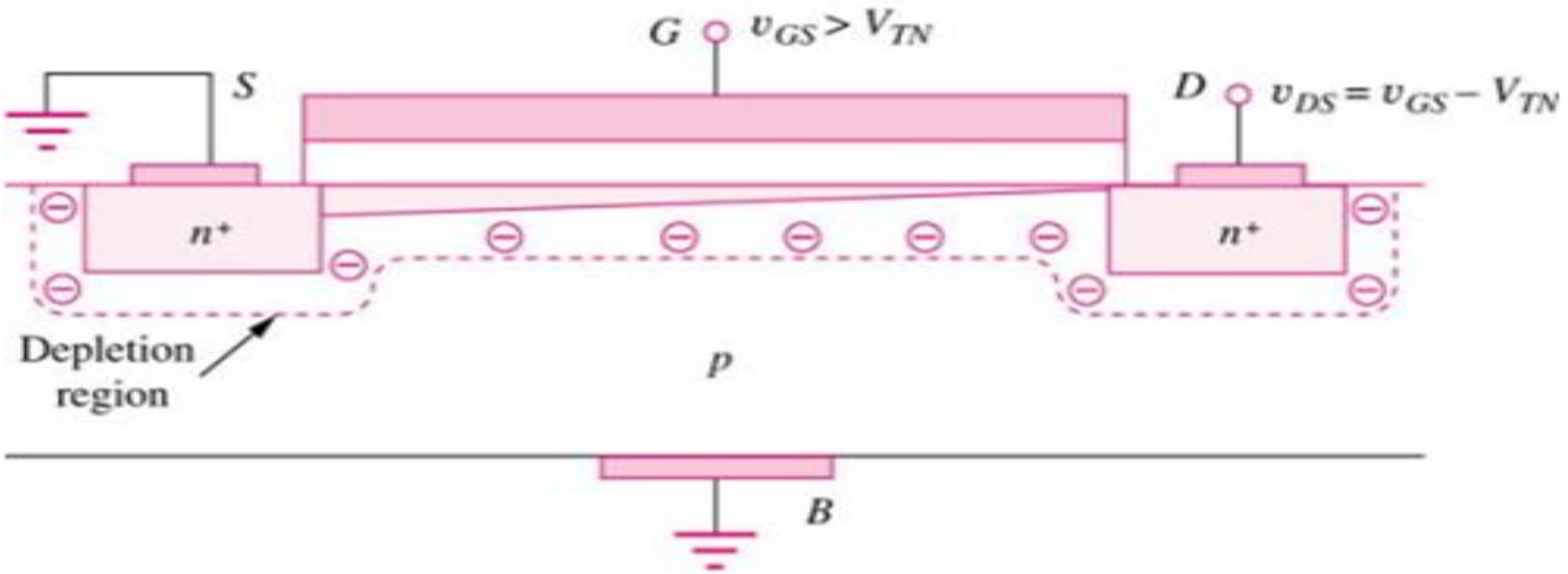

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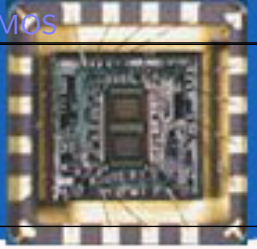
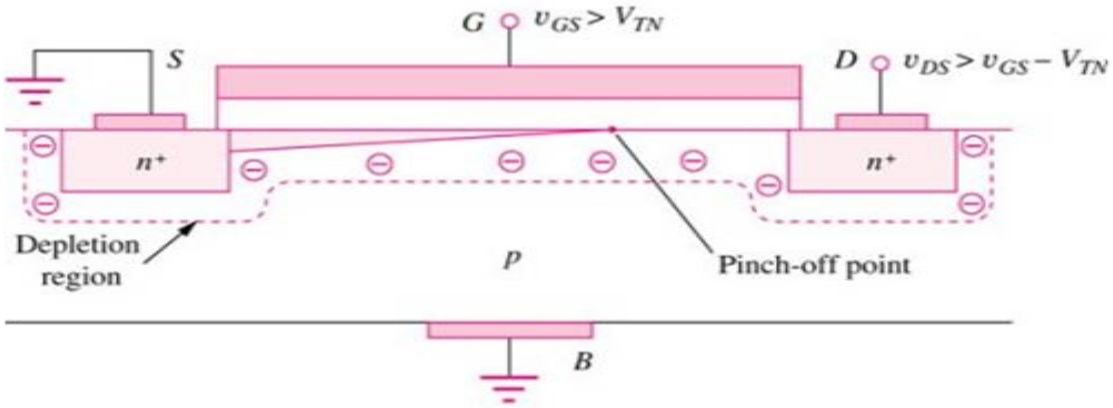
NMOS Enhancement I/V Characteristics

Saturation Region





- If v_{DS} increases above triode region limit, channel region disappears, also said to be pinched-off.
- Current saturates at constant value, independent of v_{DS}.
- Saturation region operation mostly used for analog amplification.
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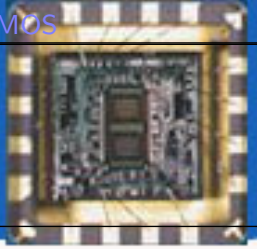

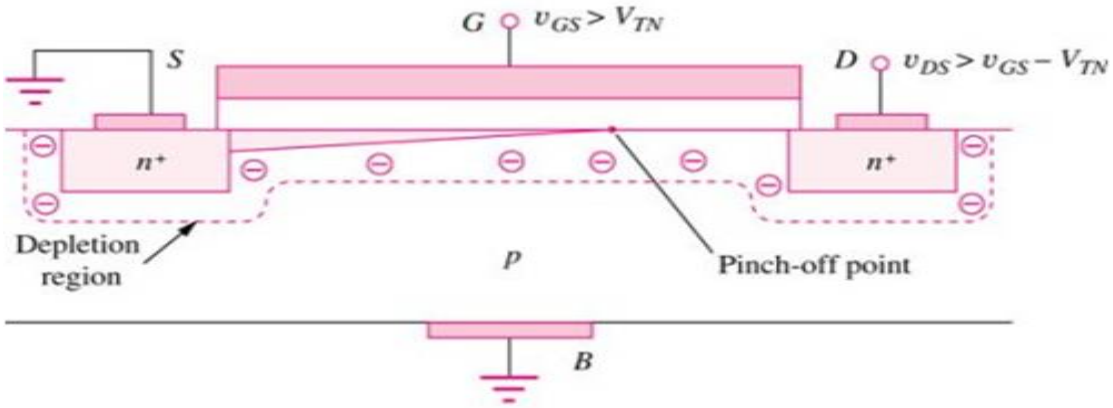

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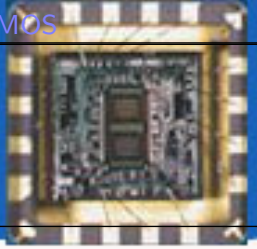

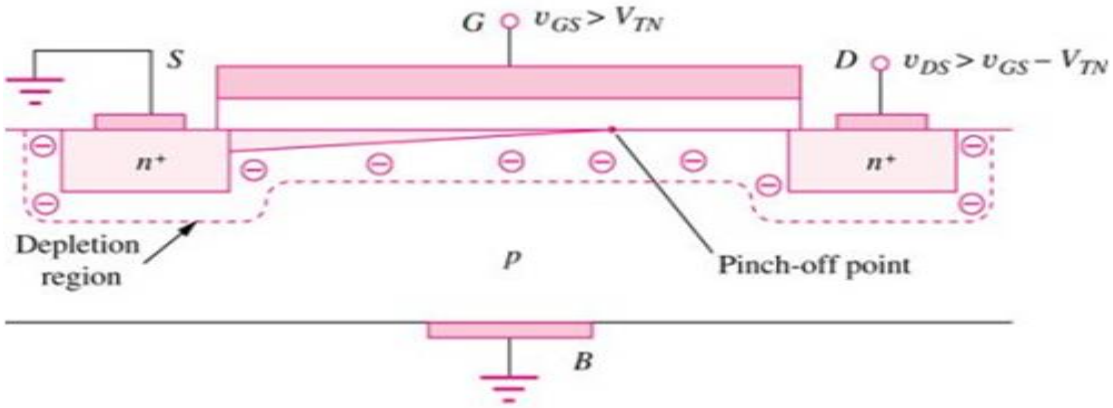

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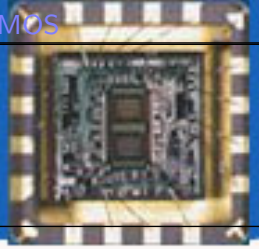

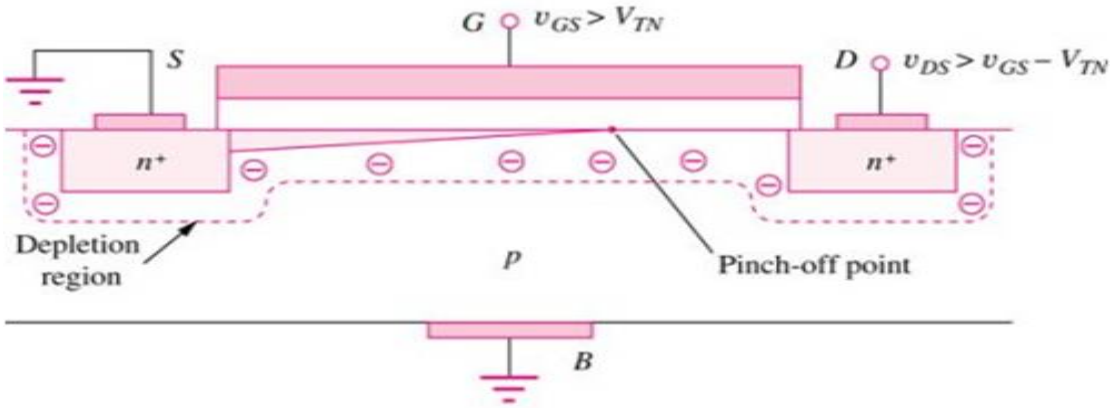

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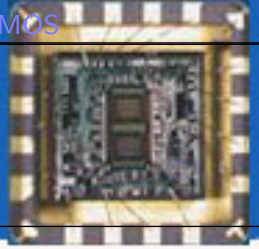

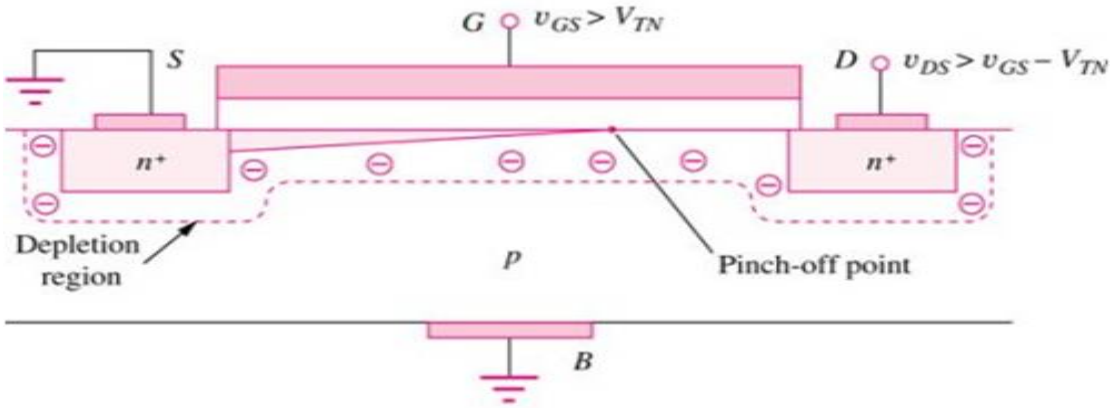

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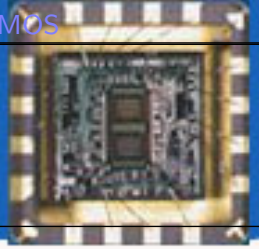
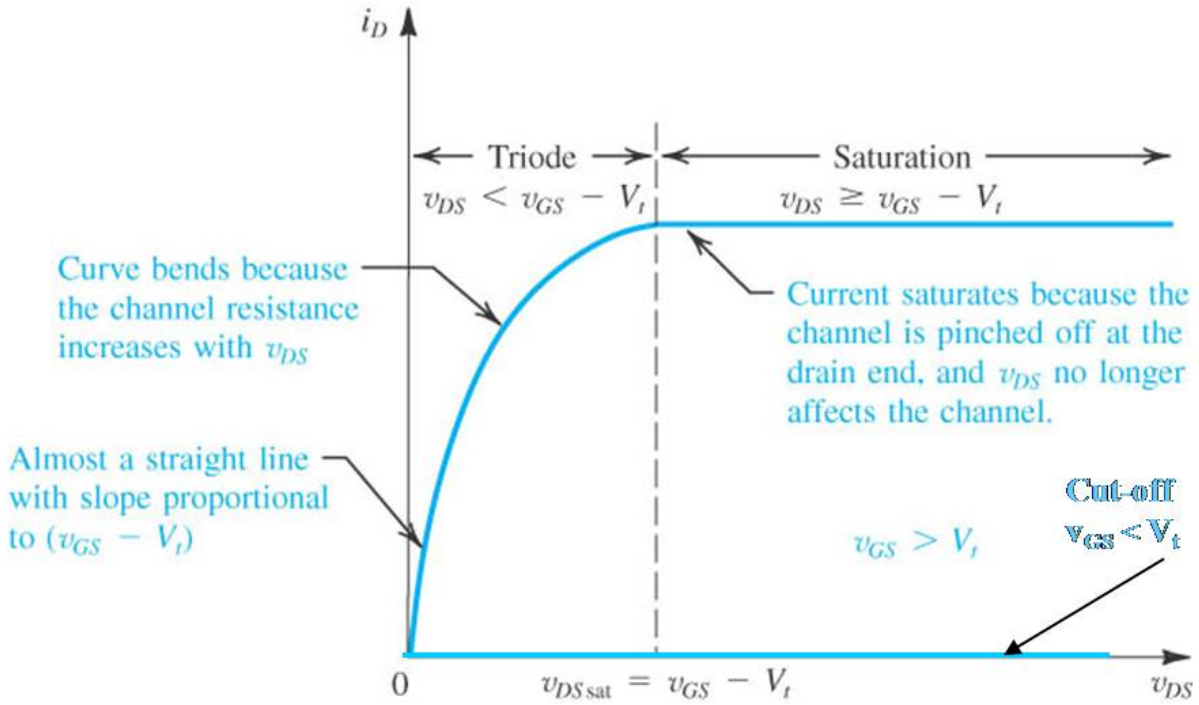
NMOS Enhancement I/V Characteristics

$I_D - V_{DS}$ Characteristics





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NMOS Enhancement I/V Characteristics

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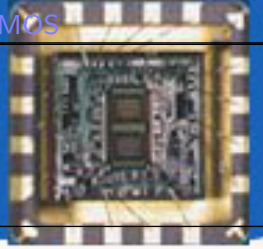

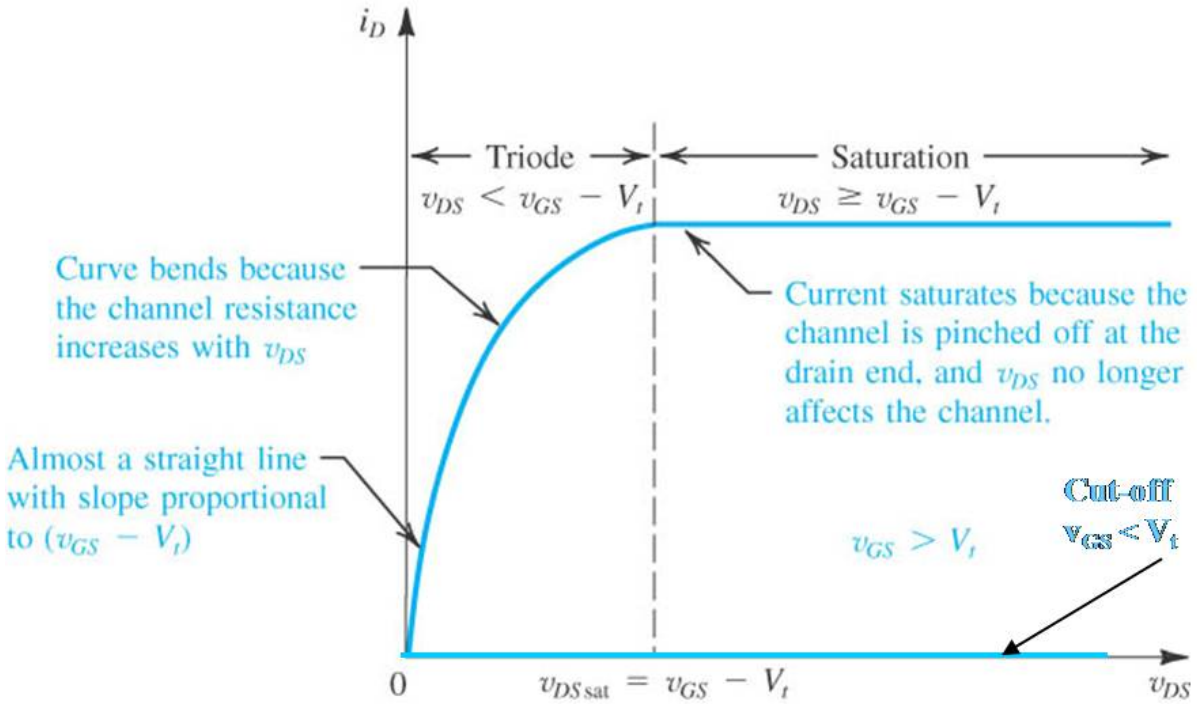

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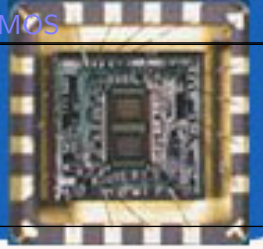
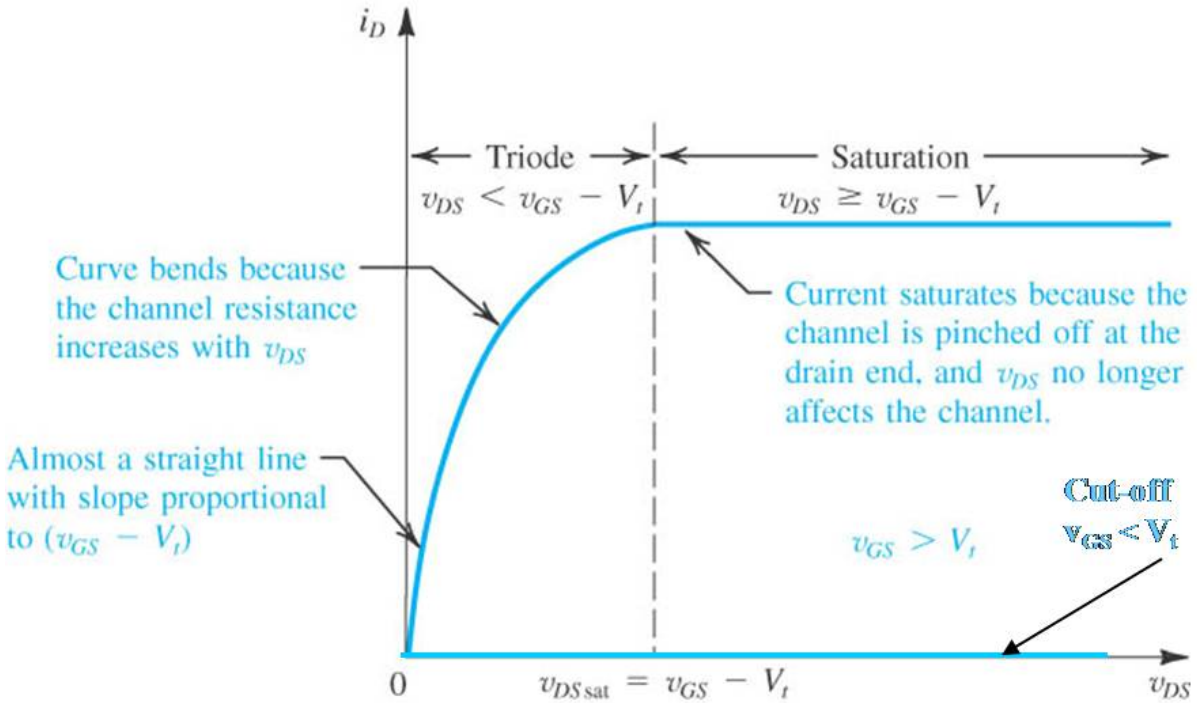
NMOS Enhancement I/V Characteristics

$I_D - V_{DS}$ Characteristics

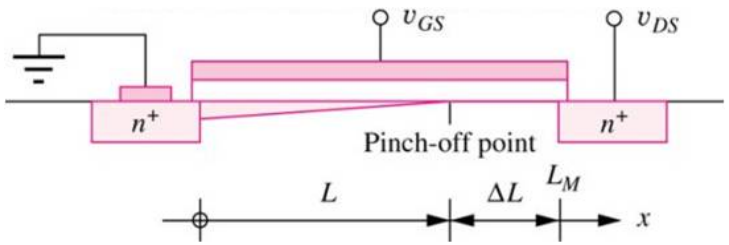




- The current is given by: $i_D = K_n' \frac{W}{L} \left(v_{GS} - V_t - \frac{v_{DS}}{2} \right) v_{DS}$ for $v_{GS} - V_t \geq v_{DS} \geq 0$
- The current is given by: $i_D = \frac{K_n'}{2} \frac{W}{L} (v_{GS} - V_t)^2$ for $v_{GS} - V_t \leq v_{DS}$

NMOS Enhancement I/V Characteristics

Channel Length Modulation

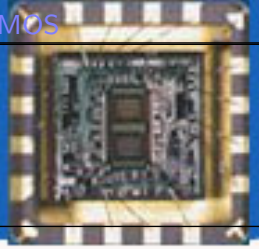


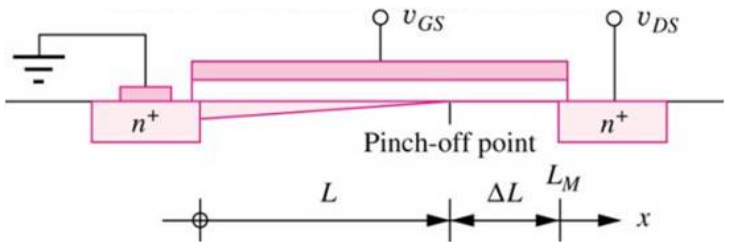
Notes

- As v_{DS} increases above v_{DSAT}, the length of the depleted channel beyond pinch-off point, ΔL, increases and actual L decreases.
- i_D increases slightly with v_{DS} instead of being constant.
- To include this effect the current at saturation may be rewritten as: $i_D = \frac{K'_n}{2}\frac{W}{L}(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})$, where λ is called channel length modulation parameter.
- In other words the output resistance at saturation will be finite equals $\frac{1}{\lambda . I_D}$.

NMOS Enhancement I/V Characteristics

Channel Length Modulation





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NMOS Enhancement I/V Characteristics

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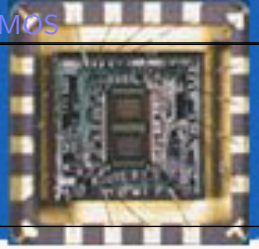

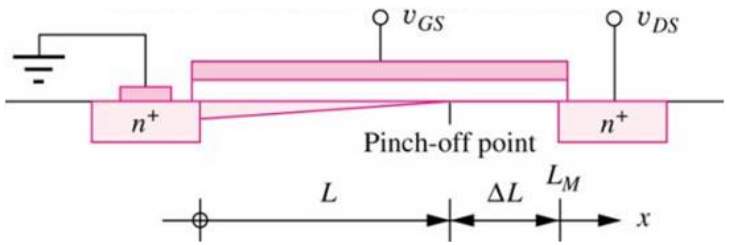

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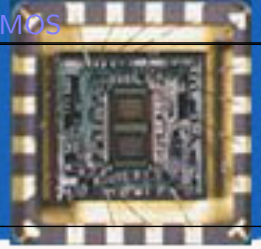
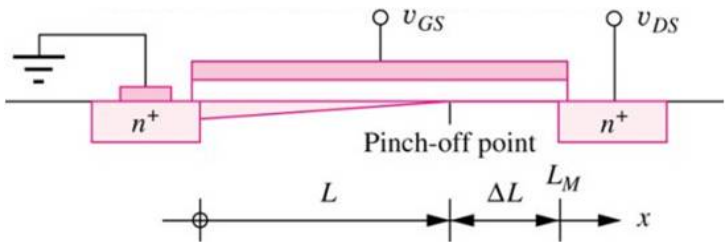
NMOS Enhancement I/V Characteristics

Channel Length Modulation





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NMOS Enhancement I/V Characteristics

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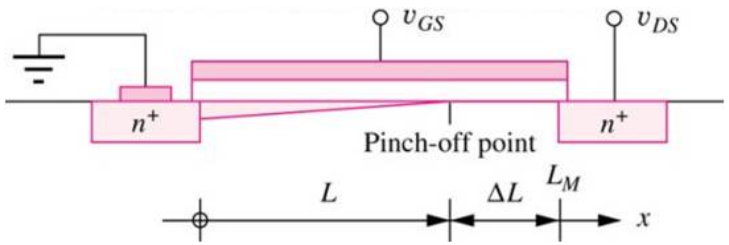

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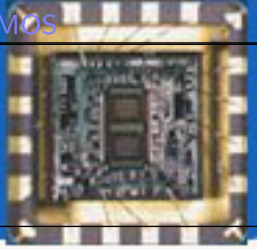
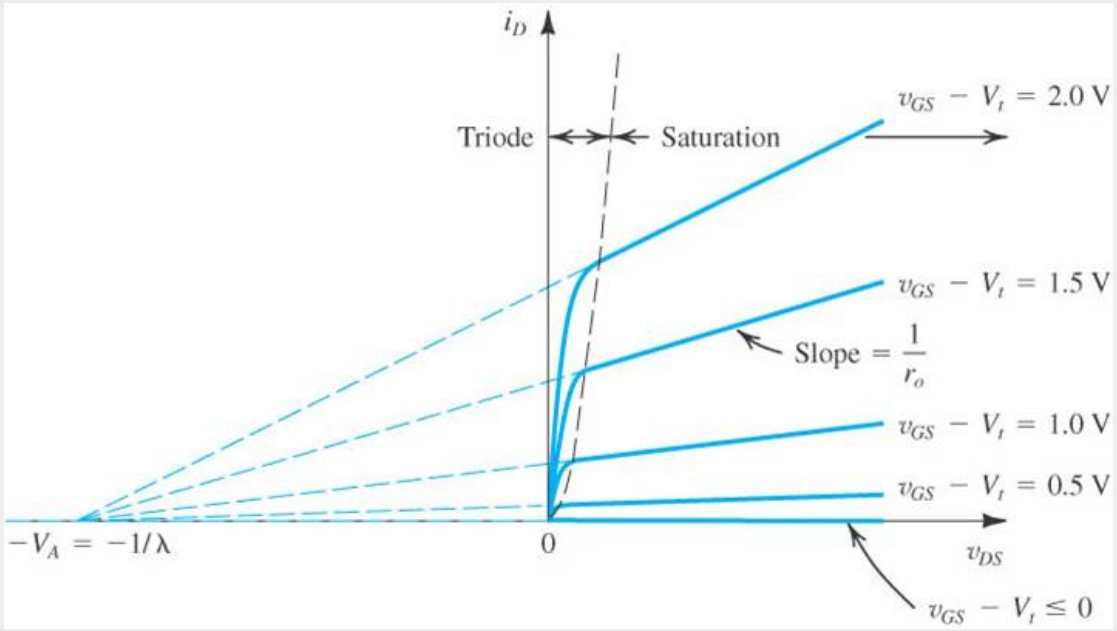
NMOS Enhancement I/V Characteristics

Effect of Channel Length Modulation on $I_D - V_{DS}$





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NMOS Enhancement I/V Characteristics

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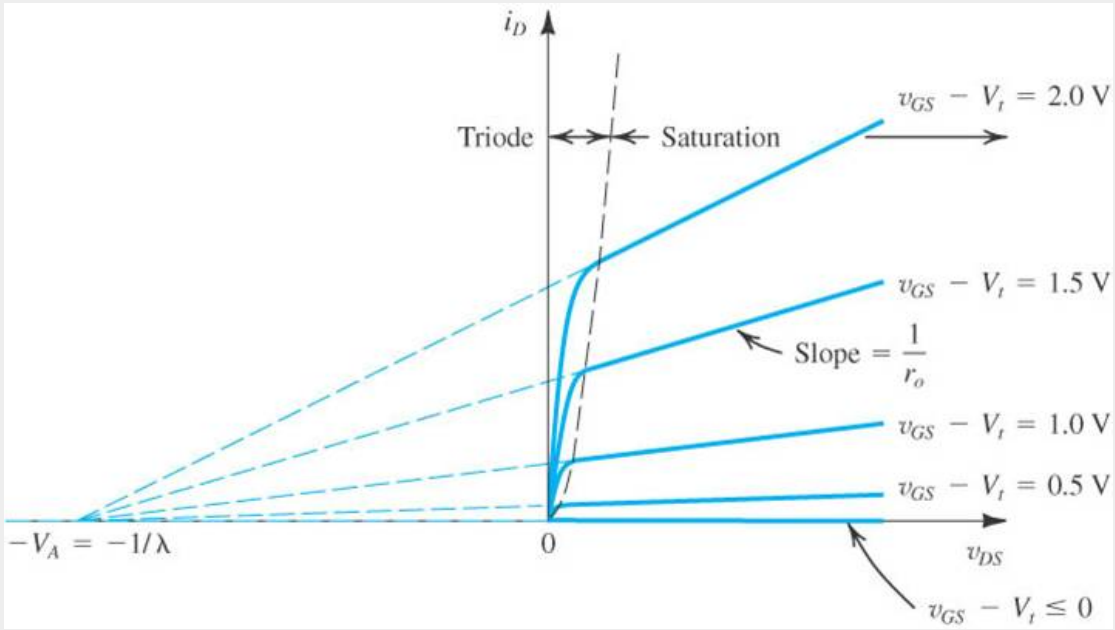

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NMOS Enhancement I/V Characteristics

Saturation Large Signal Model

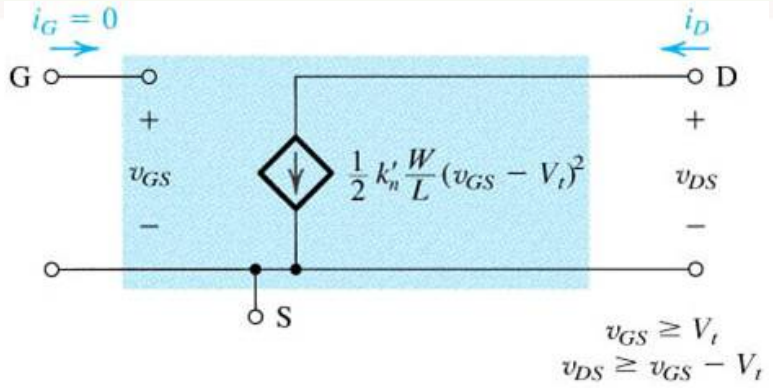


Figure: No Channel Length Modulation

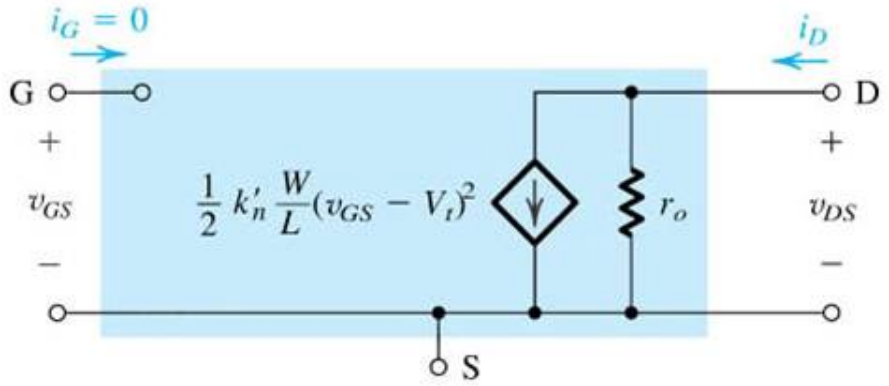
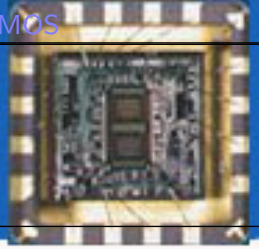
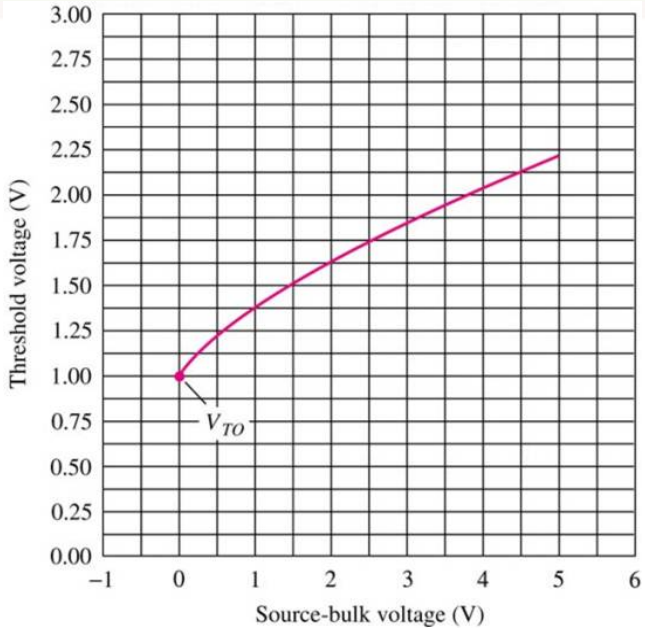


Figure: No Channel Length Modulation

NMOS Enhancement I/V Characteristics

Body Effect or Substrate Sensitivity





Notes

- Non-zero v_{SB} changes threshold voltage.
- This substrate sensitivity may be modeled by modeled by: $V_{TN} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\varphi_F} - \sqrt{2\varphi_F}\right)$ Where: V_{TO} is the zero substrate bias for V_{TN} (V), γ is the body-effect parameter ($\sqrt{V}$), and $2\varphi_F$ is the surface potential parameter (V)

NMOS Enhancement I/V Characteristics

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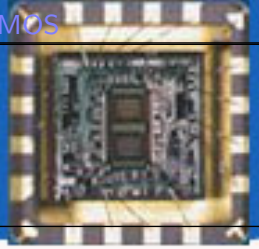

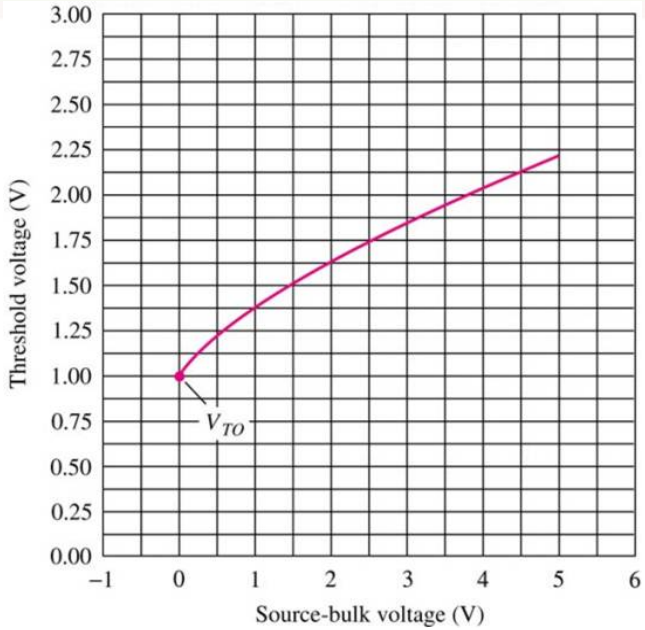

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NMOS Enhancement I/V Characteristics

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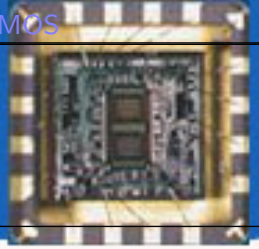

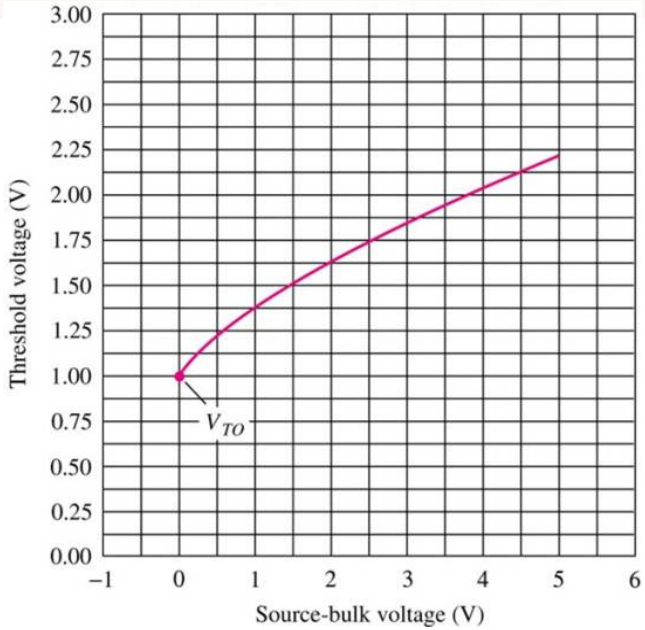

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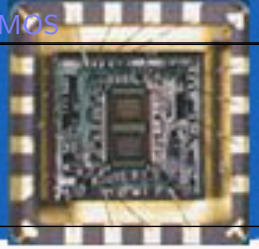
Outline



1 Enhancement NMOS Structure

2 Qualitative I/V C/Cs

3 I/V C/Cs

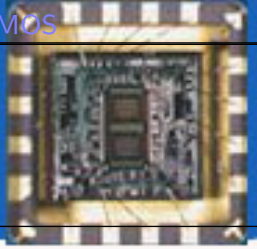
4 Depletion NMOS Transistor

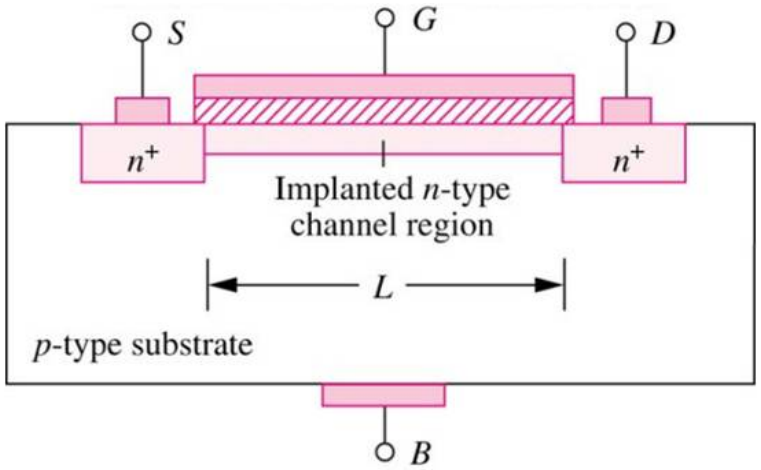
5 Enhancement PMOS Transistor

6 CMOS

NMOS Depletion Mode Transistor

Device Structure



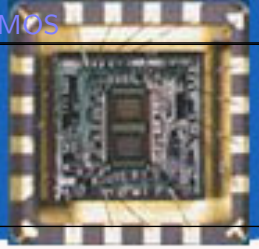


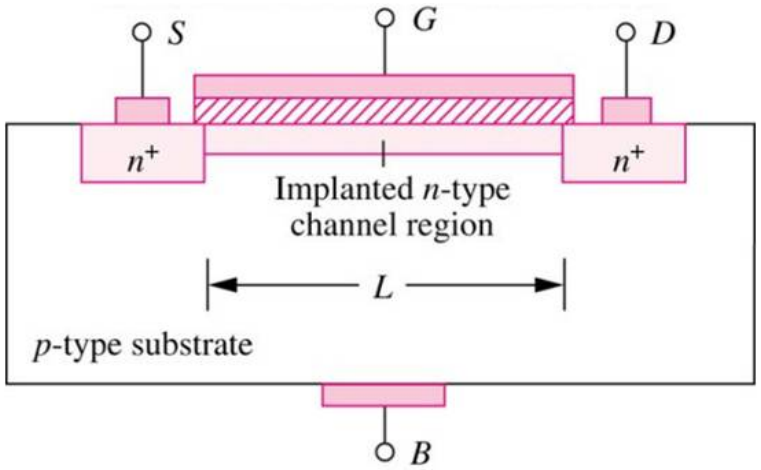
Notes

- NMOS transistors with with $V_{TN} \leq 0$
- Ion implantation process used to form a built-in n-type channel in device to connect source and drain by a resistive channel
- Non-zero drain current for $v_{GS} = 0$, negative $v_{GS} = 0$ required to turn device off.

NMOS Depletion Mode Transistor

Device Structure





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NMOS Depletion Mode Transistor

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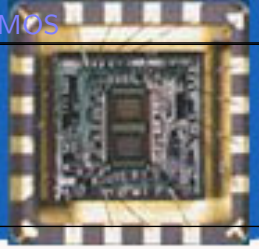

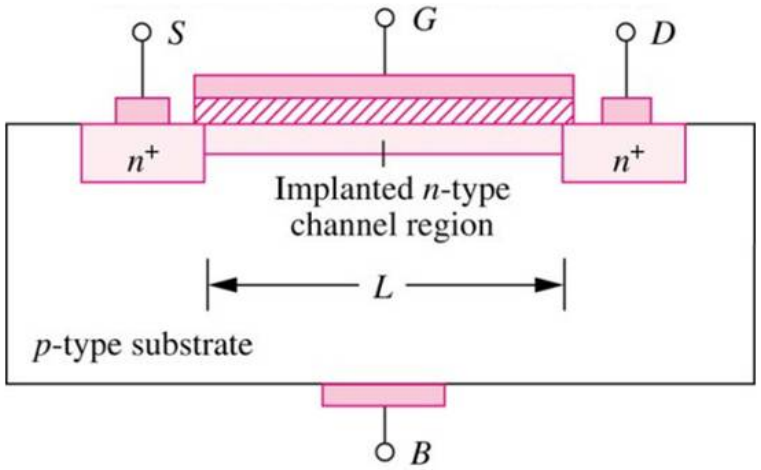

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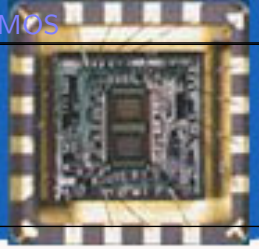

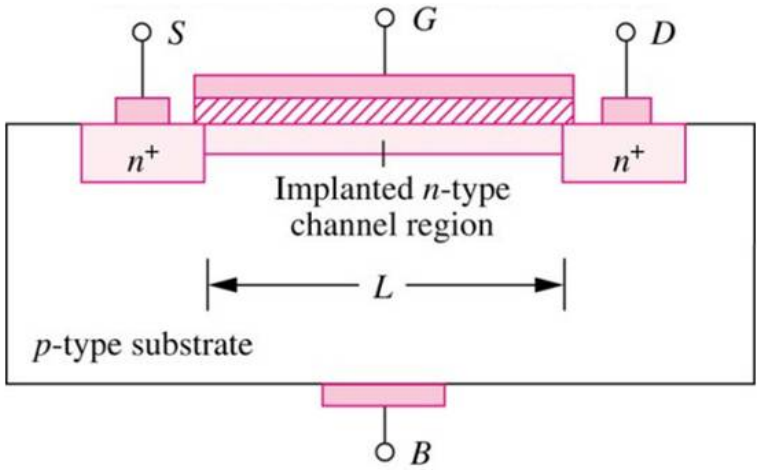

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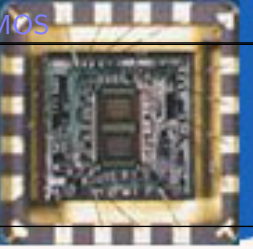
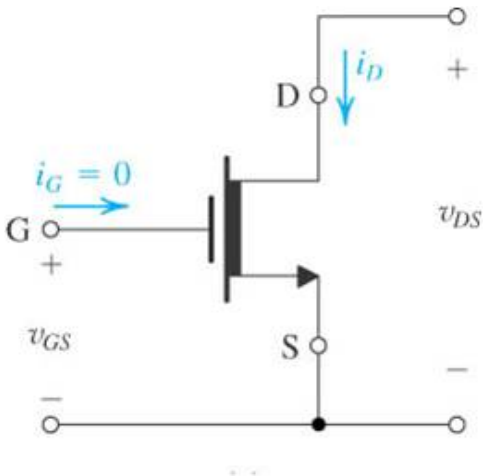
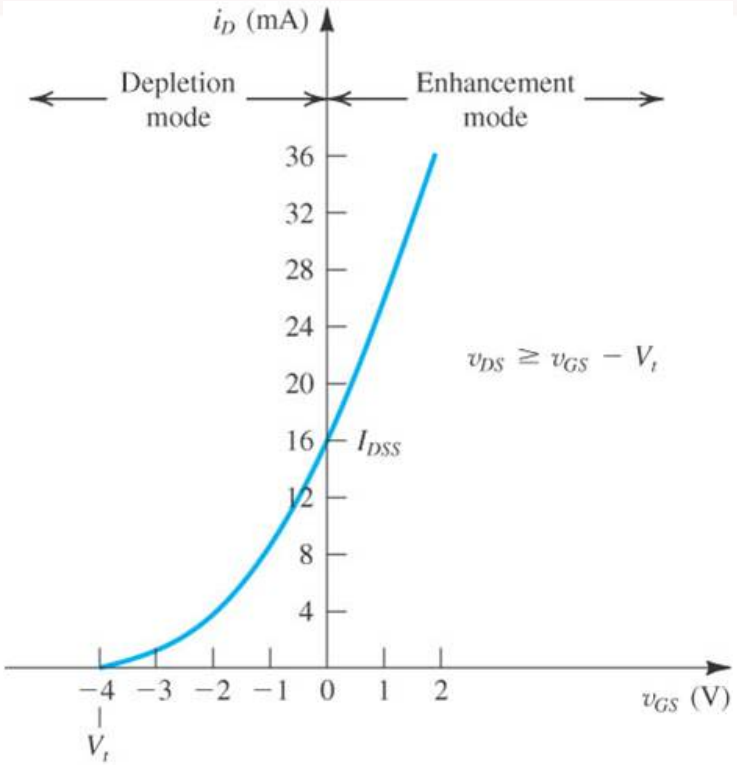
NMOS Depletion Mode Transistor

$I_D - V_{GS}$ (Input) Characteristics







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NMOS Depletion Mode Transistor

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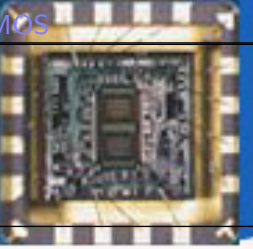

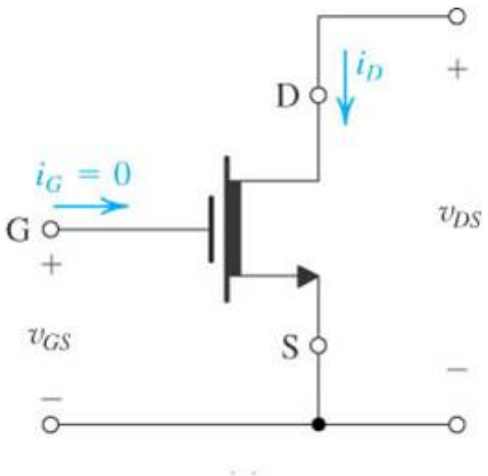

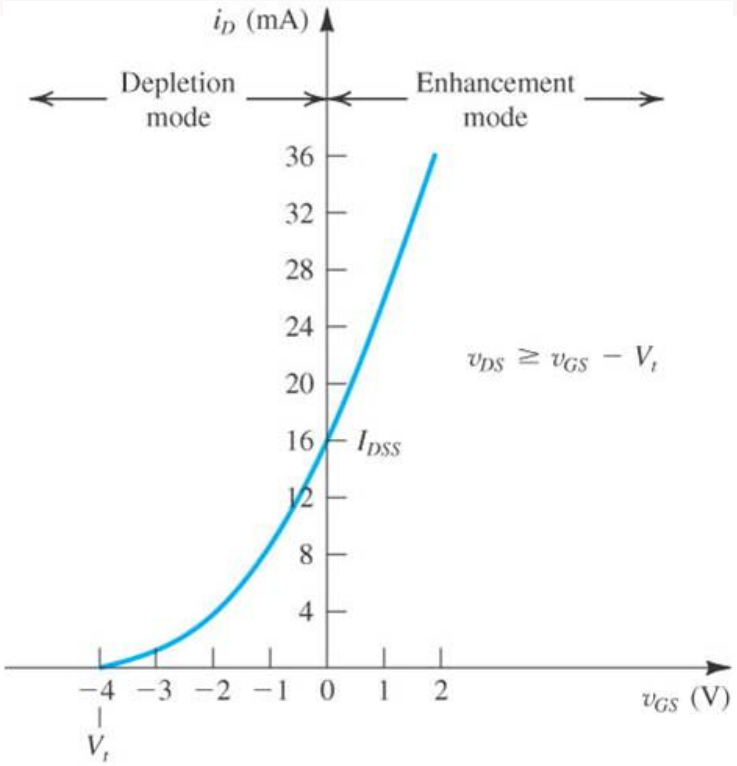

Notes

- $V_{TN} \leq 0$
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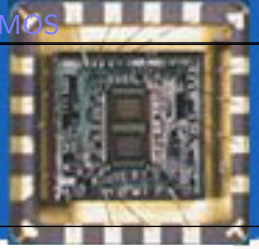
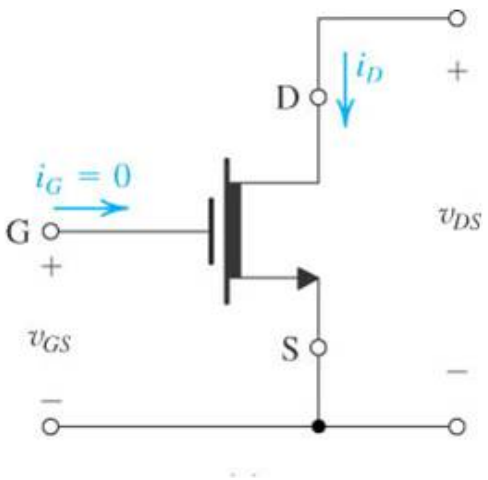
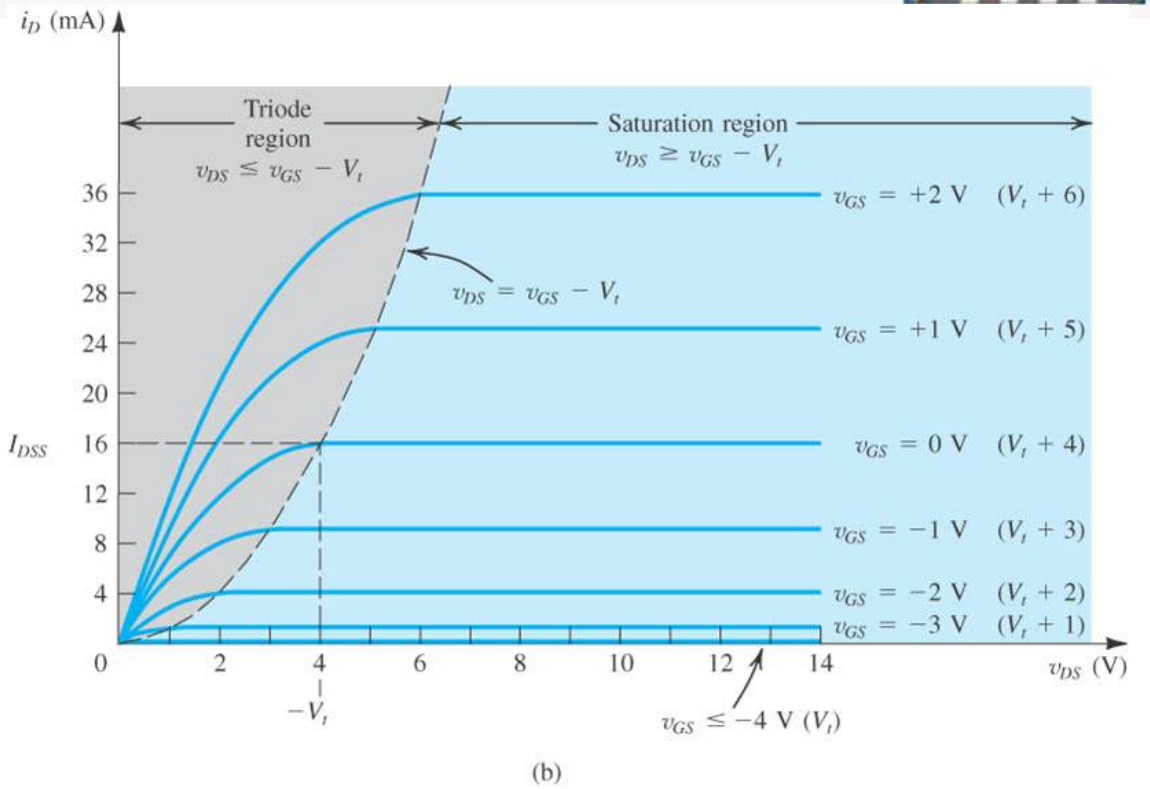
NMOS Depletion Mode Transistor

$I_D - V_{DS}$ (Output)Characteristics





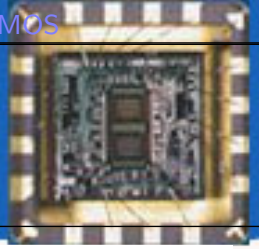


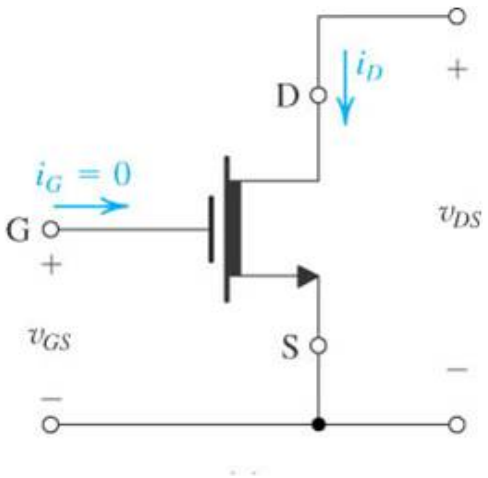
Notes

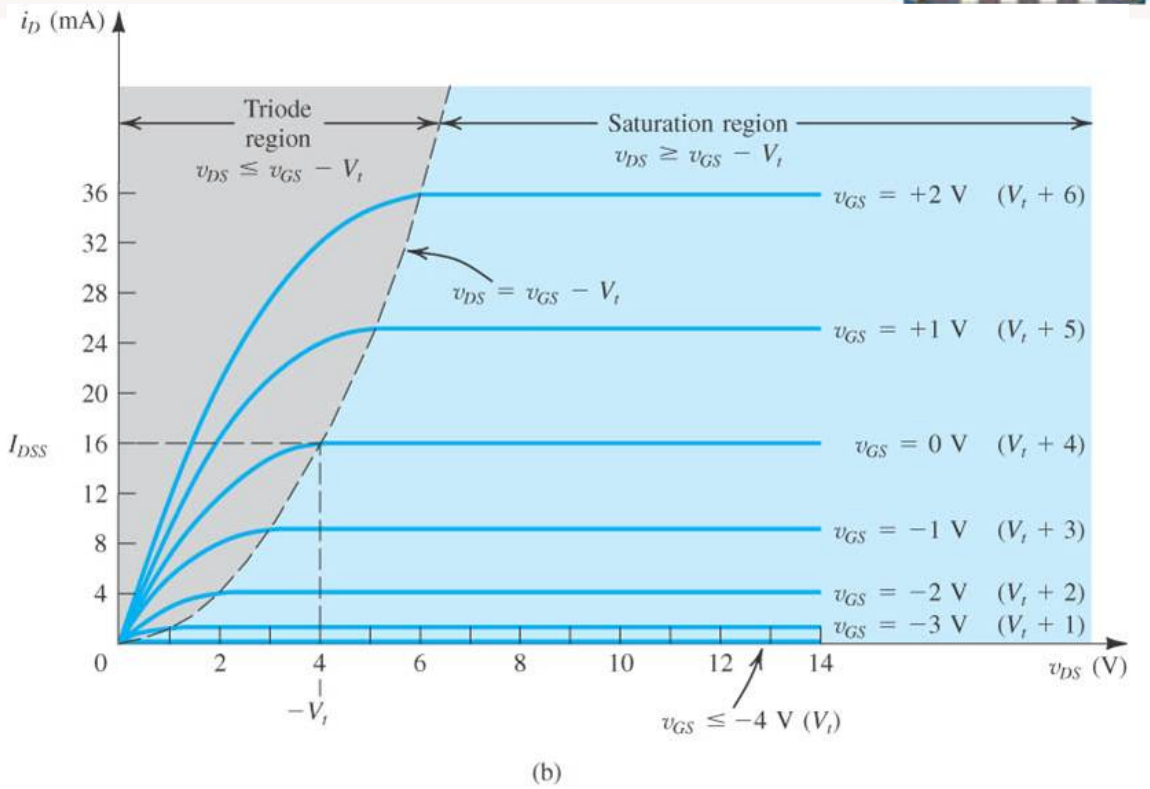
- $V_{TN} = -4$ in this example
- Non-zero drain current for $v_{GS} = 0$, negative $v_{GS} = 0$ required to turn device off.

NMOS Depletion Mode Transistor

$I_D - V_{DS}$ (Output)Characteristics





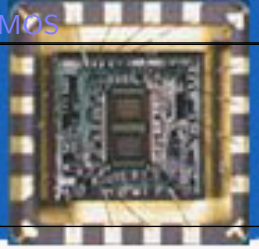


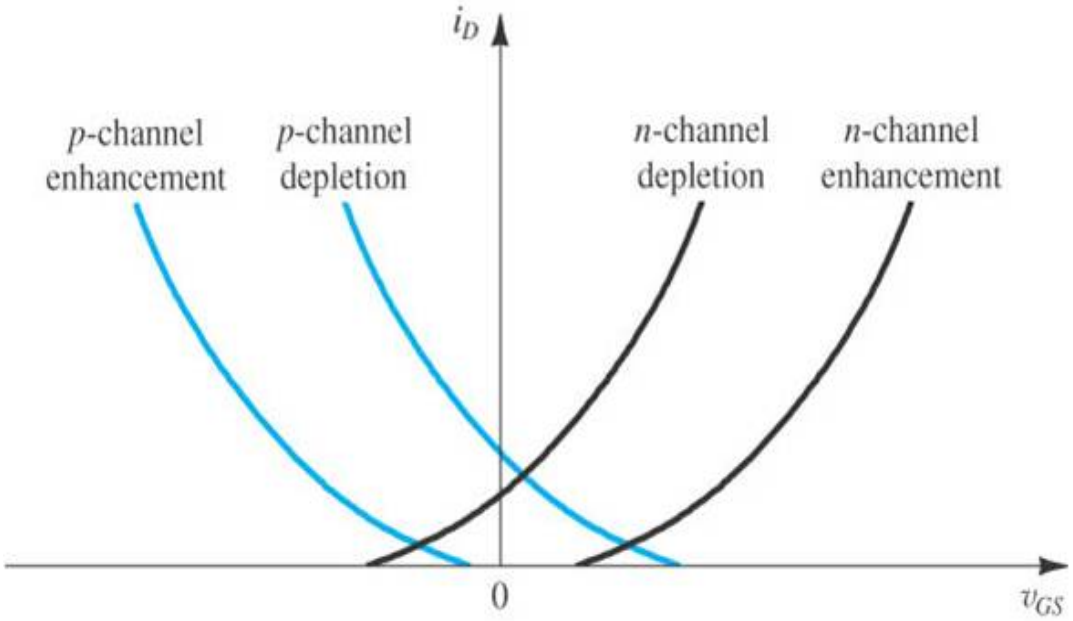
Notes

- $V_{TN} = -4$ in this example
- Non-zero drain current for $v_{GS} = 0$, negative $v_{GS} = 0$ required to turn device off.

NMOS Depletion Mode Transistor

$I_D - V_{GS}$ Characteristics Comparison



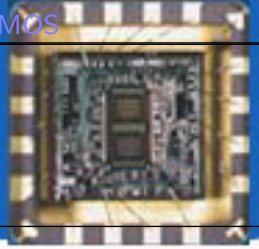


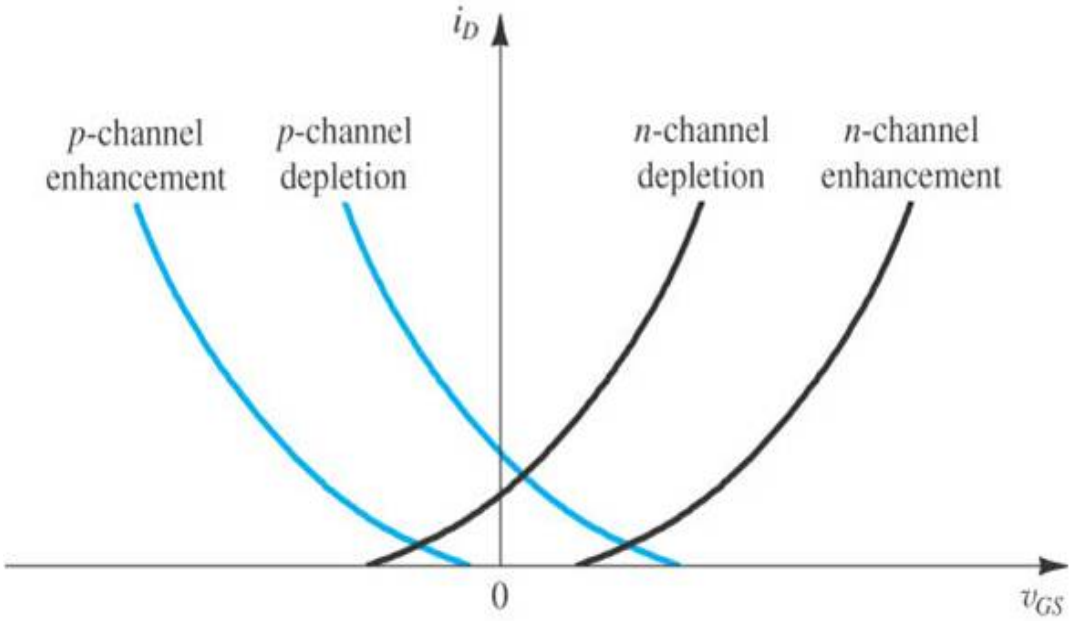
Notes

- V_t is positive for Enhancement NMOS and Depletion PMOS
- V_t is negative for Depletion NMOS and Enhancement PMOS
- Non-zero drain current for $v_{GS} = 0$ for Depletion transistors (Normally ON).

NMOS Depletion Mode Transistor

$I_D - V_{GS}$ Characteristics Comparison





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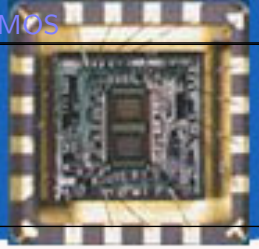
Outline



1 Enhancement NMOS Structure

2 Qualitative I/V C/Cs

3 I/V C/Cs

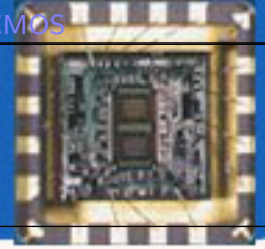
4 Depletion NMOS Transistor

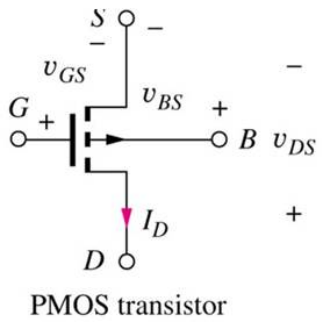
5 Enhancement PMOS Transistor

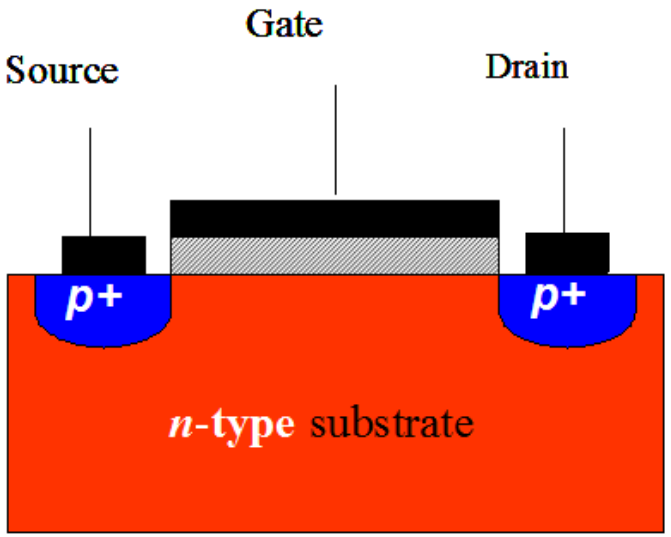
6 CMOS

Enhancement PMOS Transistor

Device Structure







Notes

- P-type source and drain regions in n-type substrate.
- $v_{GS} < 0$ required to create p-type inversion layer in channel region
- For current flow, $v_{GS} < v_{TP}$
- To maintain reverse bias on source-substrate and drain-substrate junctions, $v_{SB} < 0$ and $v_{DB} < 0$
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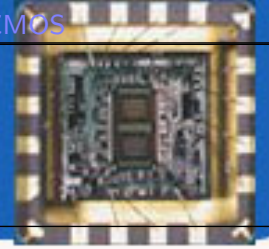
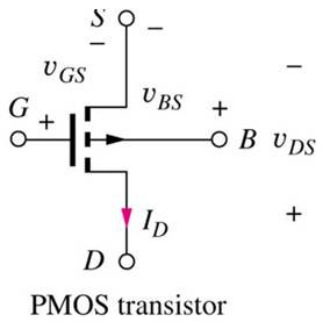
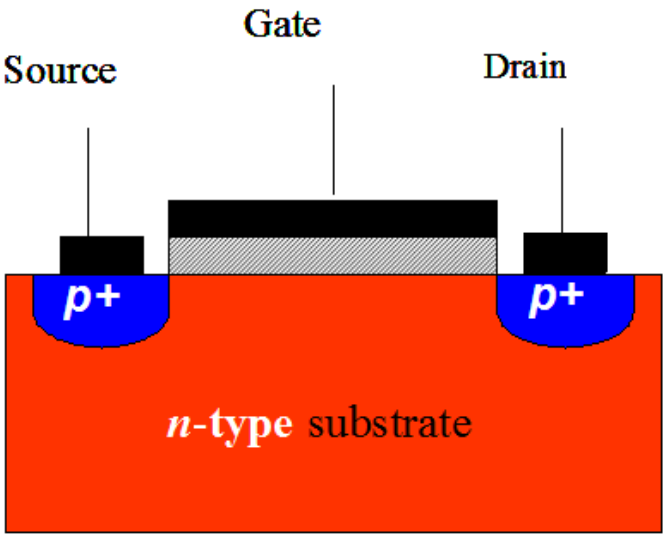
Enhancement PMOS Transistor

Device Structure







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Enhancement PMOS Transistor

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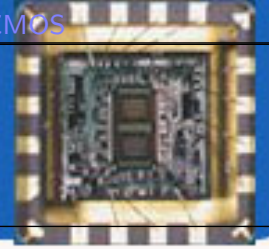
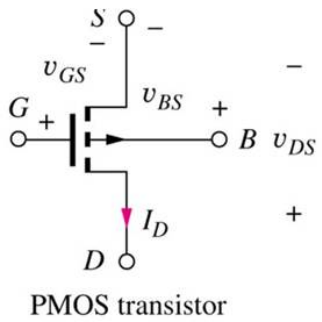
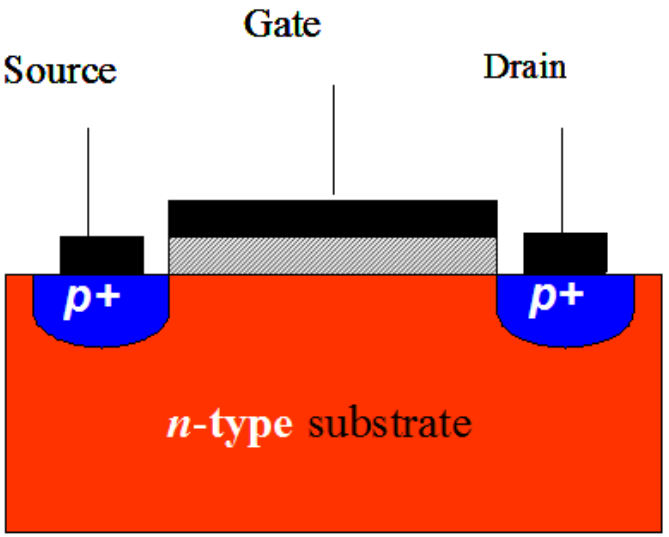




PMOS transistor



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Enhancement PMOS Transistor

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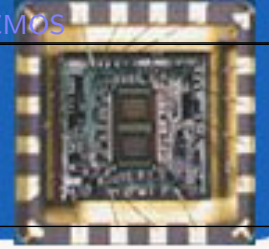

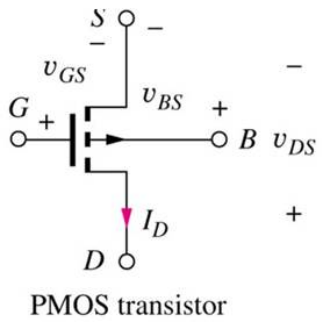

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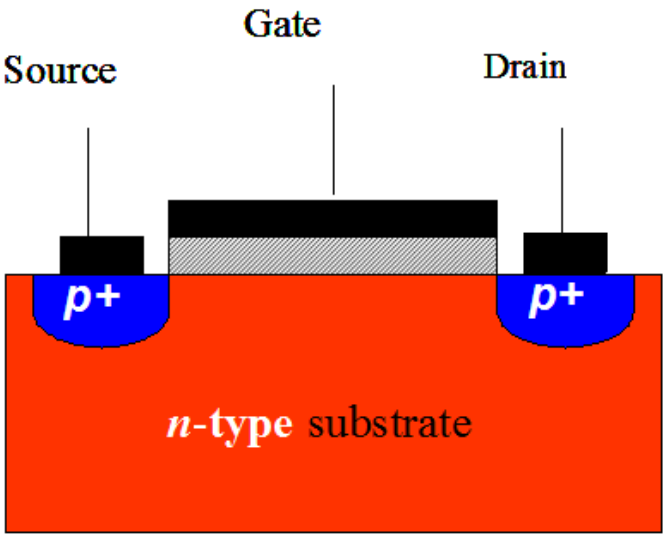

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Enhancement PMOS Transistor

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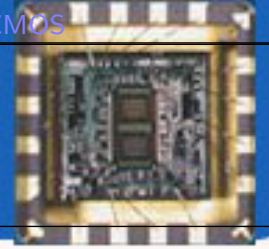

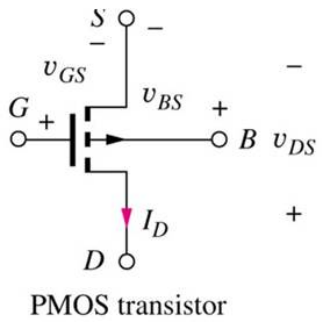

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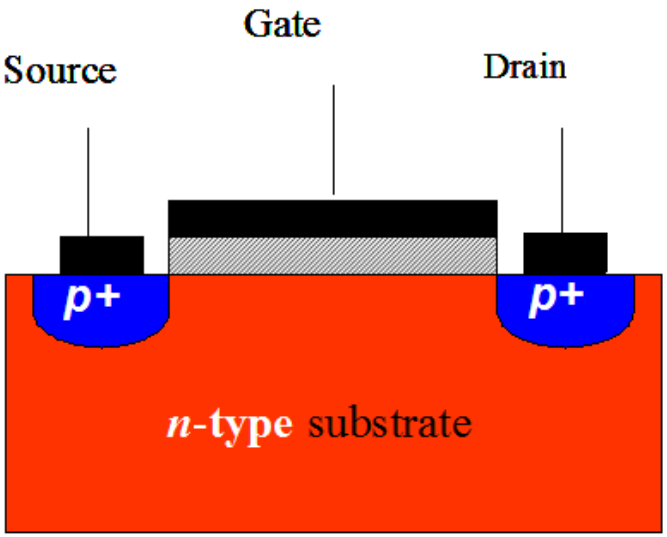

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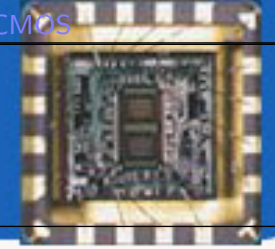

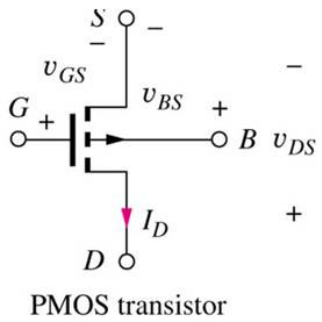

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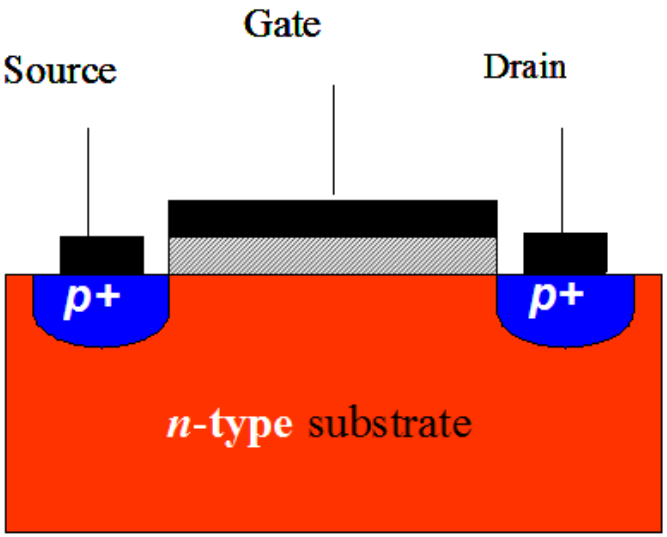

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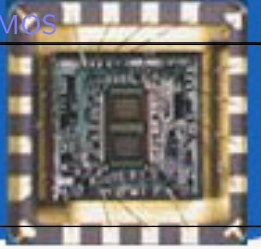
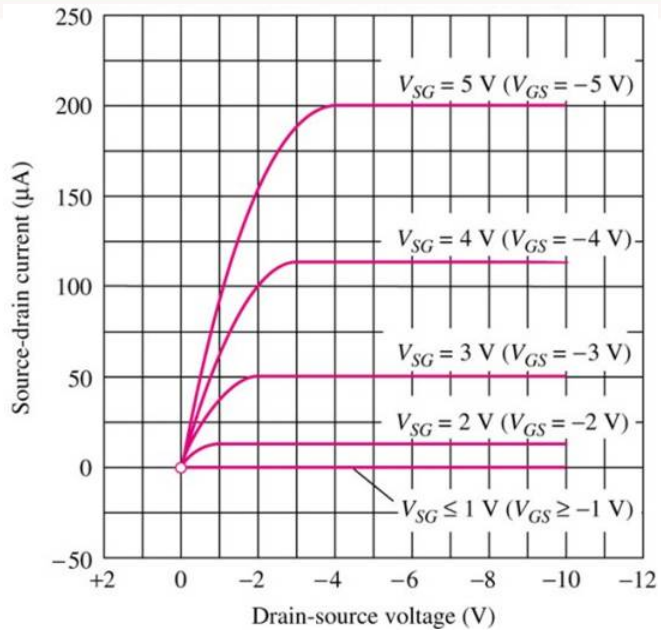
Enhancement PMOS Transistor

$I_D - V_{DS}$ (Output) Characteristics





Notes

- For $V_{GS} \geq V_{TP}$ or ($V_{SG} \leq |V_{TP}|$) the transistor is off.
- For more negative v_{GS}, drain current increases in magnitude.
- PMOS equations are the same as NMOS. However, we have to invert suffixes and use $|V_{TP}|$ instead of $|V_{TN}|$ as $|V_{TP}|$ is –ve. Also, K'_n is replaced by $K'_p = \mu_p C_{ox}$

Enhancement PMOS Transistor

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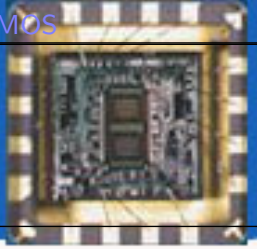

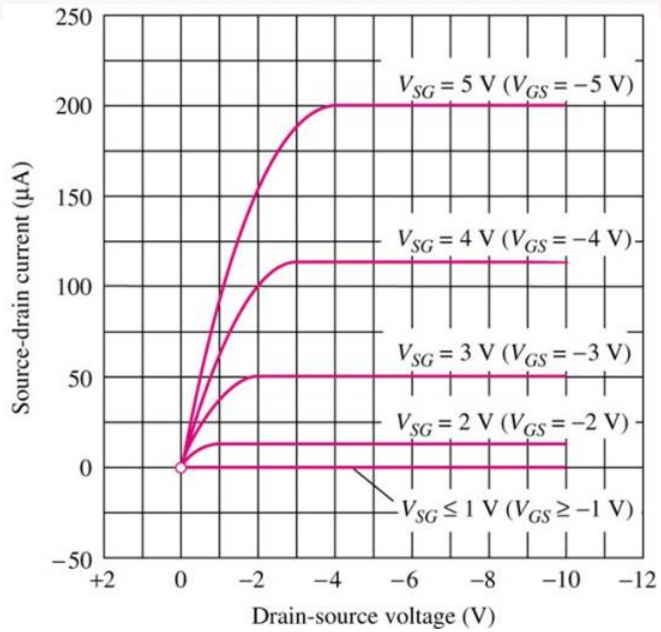

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Enhancement PMOS Transistor

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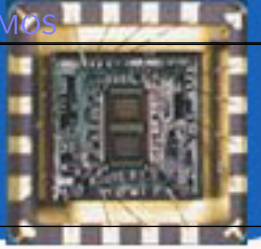

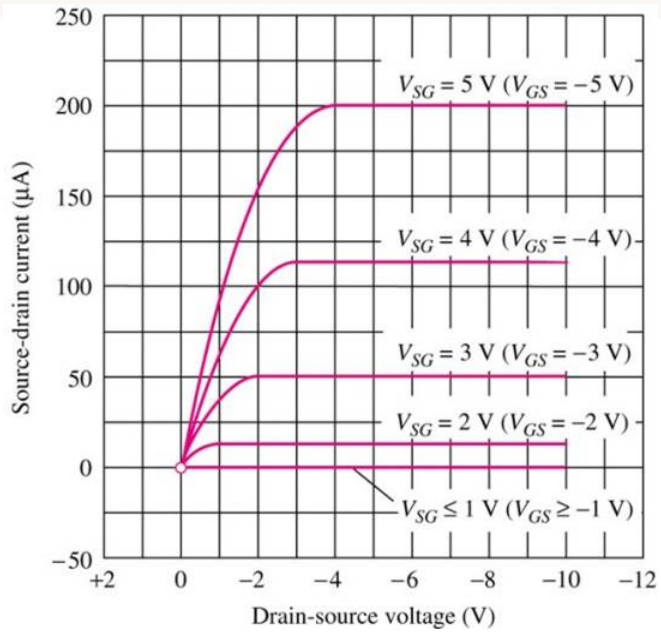

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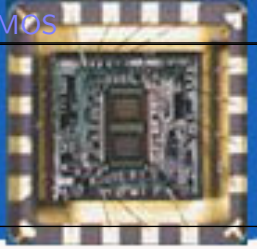
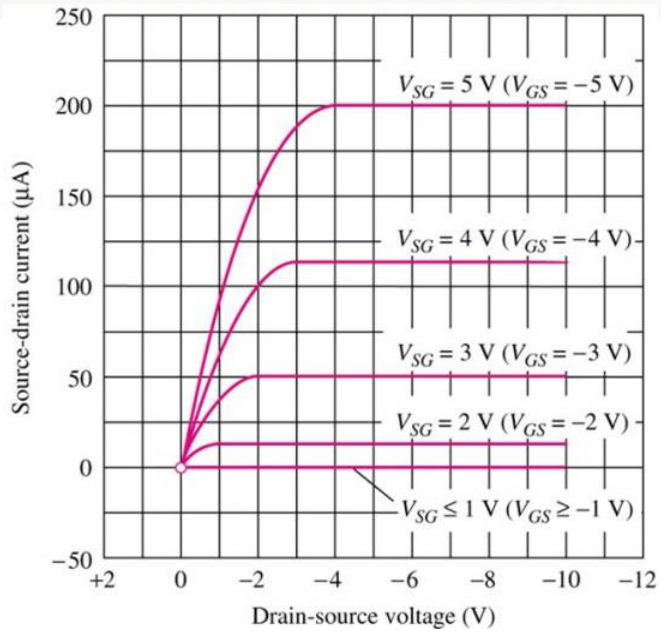
Enhancement PMOS Transistor

$I_D - V_{DS}$ (Output) Characteristics





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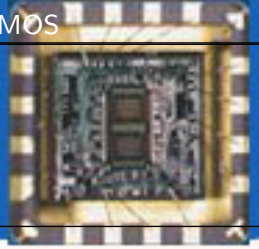

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4 Depletion NMOS Transistor

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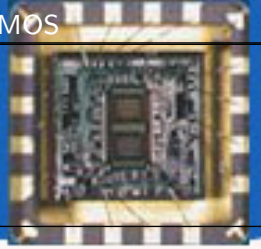
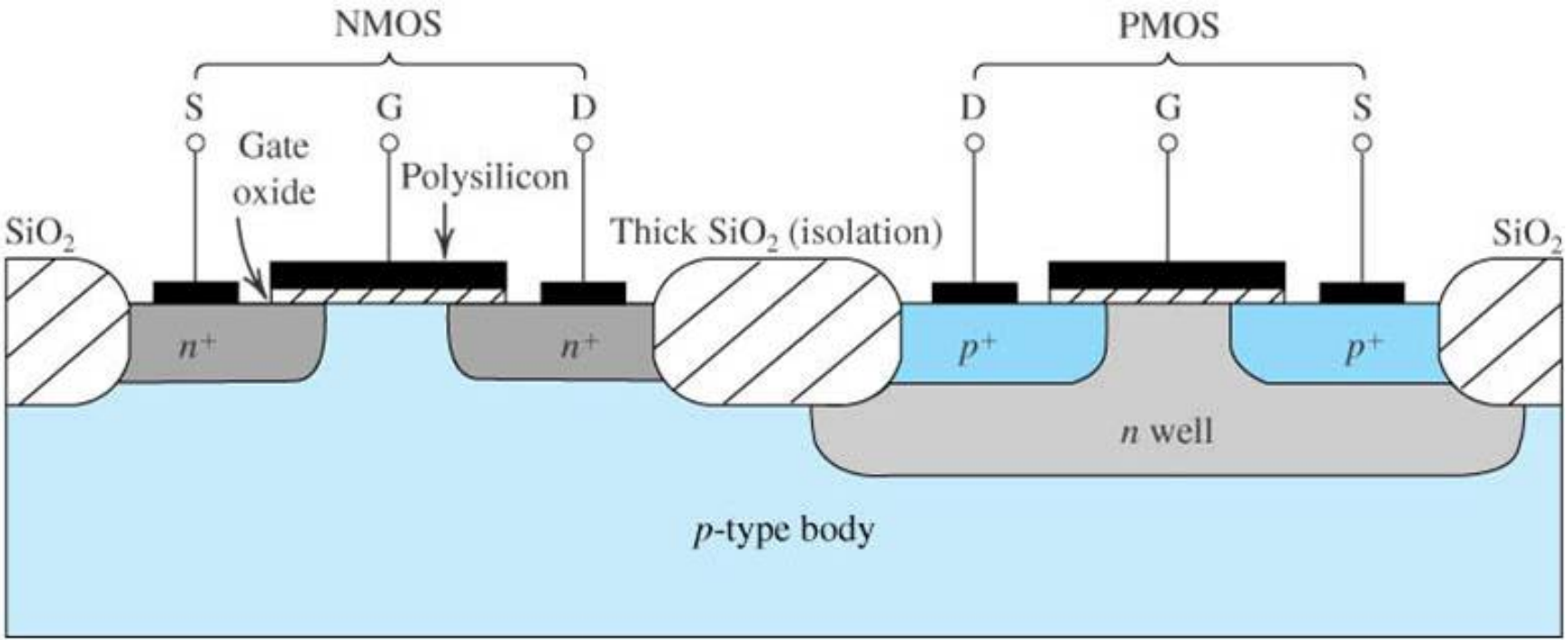
6 CMOS

Complementary MOS (CMOS)

Structure



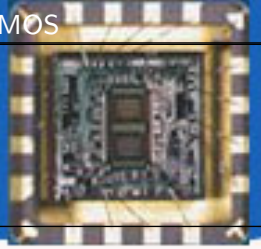


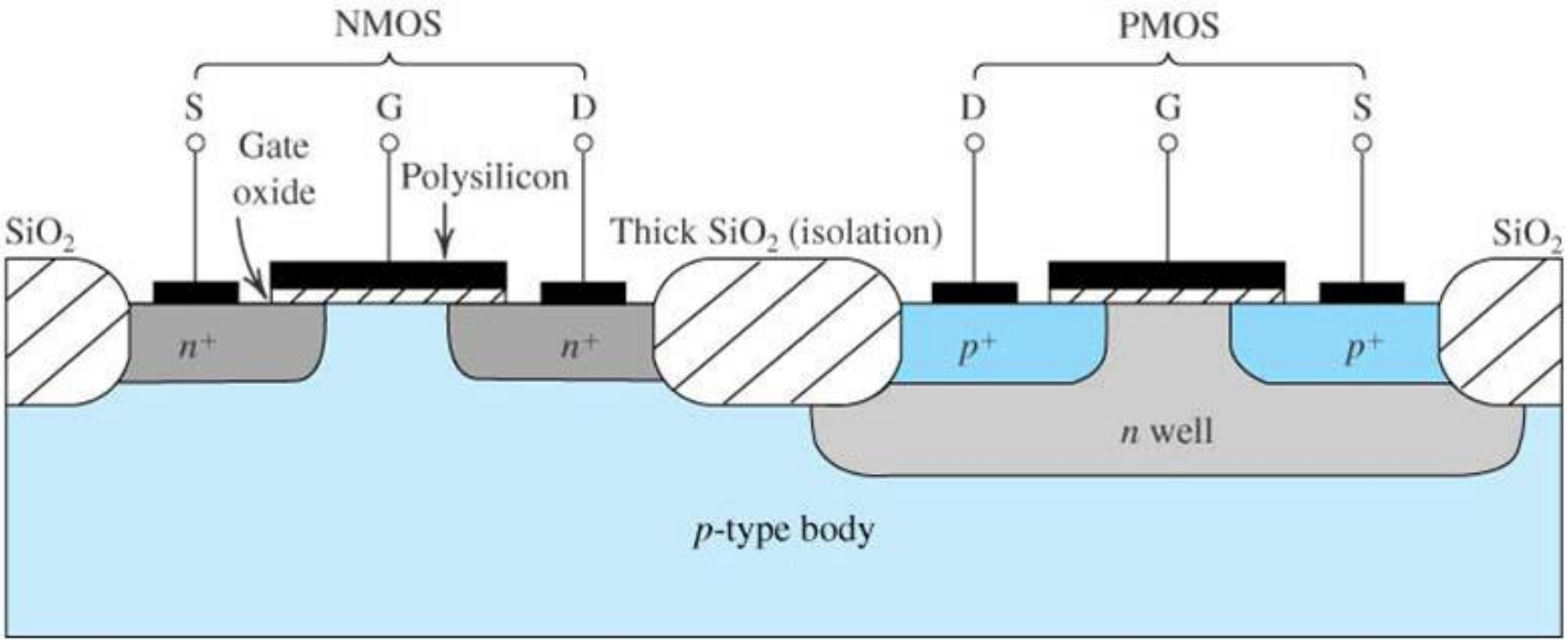
Notes

- The CMOS is consisted of NMOS and PMOS transistors.
- It is widely used in digital systems thanks to its low power dissipation

Complementary MOS (CMOS)

Structure





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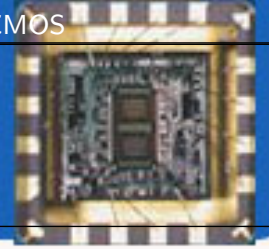

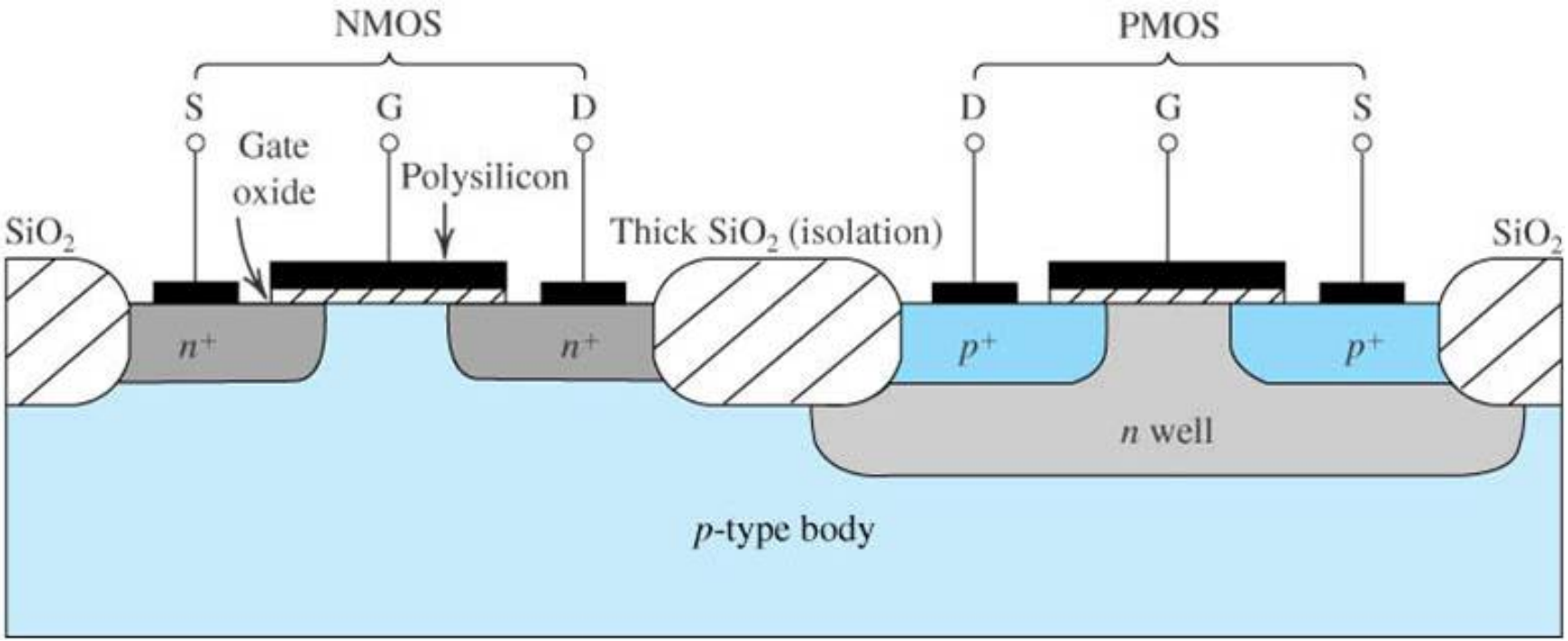

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